

Strong **IRFET**™  
**IRFP7430PbF**

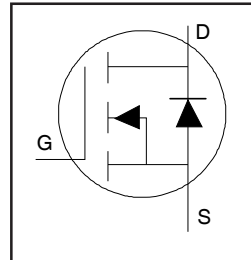
**Applications**

- Brushed Motor drive applications
- BLDC Motor drive applications
- Battery powered circuits
- Half-bridge and full-bridge topologies
- Synchronous rectifier applications
- Resonant mode power supplies
- OR-ing and redundant power switches
- DC/DC and AC/DC converters
- DC/AC Inverters

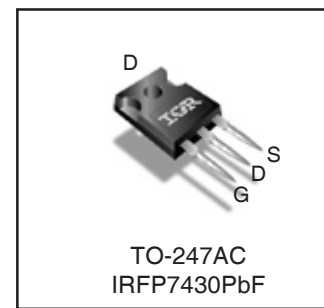
**Benefits**

- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free

HEXFET® Power MOSFET



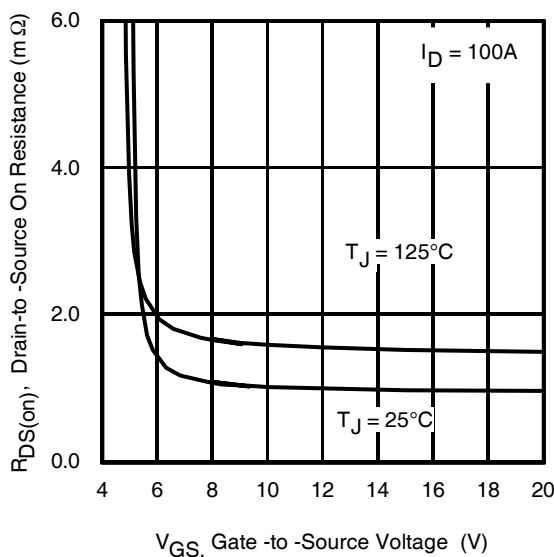
<b>V<sub>DSS</sub></b>	<b>40V</b>
<b>R<sub>DS(on)</sub> typ.</b>	<b>1.0mΩ</b>
<b>max.</b>	<b>1.3mΩ</b>
<b>I<sub>D</sub> (Silicon Limited)</b>	<b>404A</b> Ⓢ
<b>I<sub>D</sub> (Package Limited)</b>	<b>195A</b>



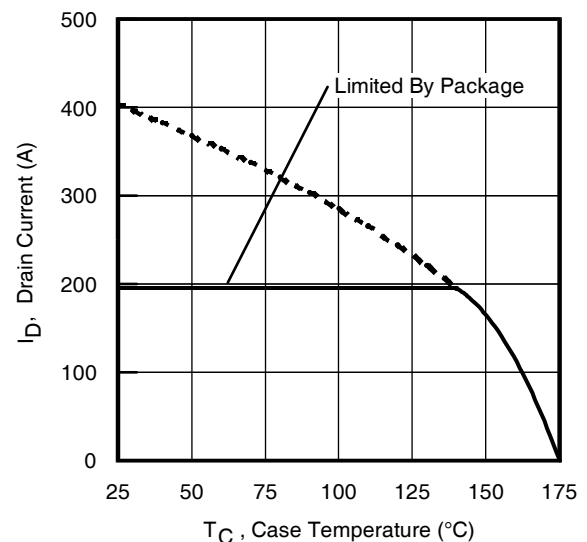
<b>G</b>	<b>D</b>	<b>S</b>
Gate	Drain	Source

**Ordering Information**

Base Part Number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
IRFP7430PbF	TO-247	Tube	50	IRFP7430PbF



**Fig 1.** Typical On-Resistance vs. Gate Voltage



**Fig 2.** Maximum Drain Current vs. Case Temperature

**Absolute Maximum Ratings**

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	404 <sup>①</sup>	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	286 <sup>①</sup>	
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Wire Bond Limited)	195	
$I_{DM}$	Pulsed Drain Current <sup>②</sup>	1524	
$P_D @ T_C = 25^\circ\text{C}$	Maximum Power Dissipation	366	W
	Linear Derating Factor	2.4	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$T_J$ $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw	10lbf·in (1.1N·m)	

**Avalanche Characteristics**

$E_{AS}$ (Thermally limited)	Single Pulse Avalanche Energy <sup>③</sup>	722	mJ
$E_{AS}$ (tested)	Single Pulse Avalanche Energy Tested Value <sup>③</sup>	1360	
$I_{AR}$	Avalanche Current <sup>④</sup>	See Fig. 14, 15, 22a, 22b	A
$E_{AR}$	Repetitive Avalanche Energy <sup>④</sup>		mJ

**Thermal Resistance**

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case <sup>⑤</sup>	—	0.41	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient	—	40	

**Static @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)**

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40	—	—	V	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.014	—	V/°C	Reference to $25^\circ\text{C}, I_D = 1.0\text{mA}$ <sup>②</sup>
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	1.0	1.3	mΩ	$V_{GS} = 10\text{V}, I_D = 100\text{A}$ <sup>⑤</sup>
			1.2	—	mΩ	$V_{GS} = 6.0\text{V}, I_D = 50\text{A}$ <sup>⑤</sup>
$V_{GS(th)}$	Gate Threshold Voltage	2.2	—	3.9	V	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	1.0	μA	$V_{DS} = 40\text{V}, V_{GS} = 0\text{V}$
				150	μA	$V_{DS} = 40\text{V}, V_{GS} = 0\text{V}, T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20\text{V}$
	Gate-to-Source Reverse Leakage	—	—	-100	nA	$V_{GS} = -20\text{V}$
$R_G$	Internal Gate Resistance	—	2.1	—	Ω	

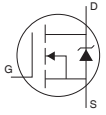
**Notes:**

- ① Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 195A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements. (Refer to AN-1140)
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ Limited by  $T_{Jmax}$ , starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.14\text{mH}$   
 $R_G = 50\Omega, I_{AS} = 100\text{A}, V_{GS} = 10\text{V}$ .
- ④  $I_{SD} \leq 100\text{A}$ ,  $di/dt \leq 990\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_J \leq 175^\circ\text{C}$ .
- ⑤ Pulse width  $\leq 400\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ⑥  $C_{oss}$  eff. (TR) is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑦  $C_{oss}$  eff. (ER) is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑧ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑨  $R_{\theta}$  is measured at  $T_J$  approximately  $90^\circ\text{C}$ .
- ⑩ This value determined from sample failure population, starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.14\text{mH}$ ,  $R_G = 50\Omega, I_{AS} = 100\text{A}, V_{GS} = 10\text{V}$ .

**Dynamic @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)**

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$g_{fs}$	Forward Transconductance	150	—	—	S	$V_{DS} = 10V, I_D = 100A$
$Q_g$	Total Gate Charge	—	300	460	nC	$I_D = 100A$ $V_{DS} = 20V$ $V_{GS} = 10V$ ⑤
$Q_{gs}$	Gate-to-Source Charge	—	77	—		
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	98	—		
$Q_{sync}$	Total Gate Charge Sync. ( $Q_g - Q_{gd}$ )	—	202	—		
$t_{d(on)}$	Turn-On Delay Time	—	32	—	ns	$V_{DD} = 20V$ $I_D = 30A$ $R_G = 2.7\Omega$ $V_{GS} = 10V$ ⑤
$t_r$	Rise Time	—	105	—		
$t_{d(off)}$	Turn-Off Delay Time	—	160	—		
$t_f$	Fall Time	—	100	—		
$C_{iss}$	Input Capacitance	—	14240	—	pF	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1.0\text{ MHz}$
$C_{oss}$	Output Capacitance	—	2130	—		
$C_{rss}$	Reverse Transfer Capacitance	—	1460	—		
$C_{oss\text{ eff. (ER)}}$	Effective Output Capacitance (Energy Related) ②	—	2605	—		
$C_{oss\text{ eff. (TR)}}$	Effective Output Capacitance (Time Related) ⑥	—	2920	—		

**Diode Characteristics**

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	376 ①	A	MOSFET symbol showing the integral reverse p-n junction diode. 
$I_{SM}$	Pulsed Source Current (Body Diode) ②	—	—	1576	A	
$V_{SD}$	Diode Forward Voltage	—	0.86	1.2	V	$T_J = 25^\circ\text{C}, I_S = 100A, V_{GS} = 0V$ ⑤
$dv/dt$	Peak Diode Recovery ④	—	2.7	—	V/ns	$T_J = 175^\circ\text{C}, I_S = 100A, V_{DS} = 40V$
$t_{rr}$	Reverse Recovery Time	—	52	—	ns	$V_R = 34V,$ $I_F = 100A$ $di/dt = 100A/\mu s$ ⑤
		—	52	—		
$Q_{rr}$	Reverse Recovery Charge	—	97	—	nC	$T_J = 25^\circ\text{C}$ $T_J = 125^\circ\text{C}$
		—	97	—		
$I_{RRM}$	Reverse Recovery Current	—	2.3	—	A	$T_J = 25^\circ\text{C}$

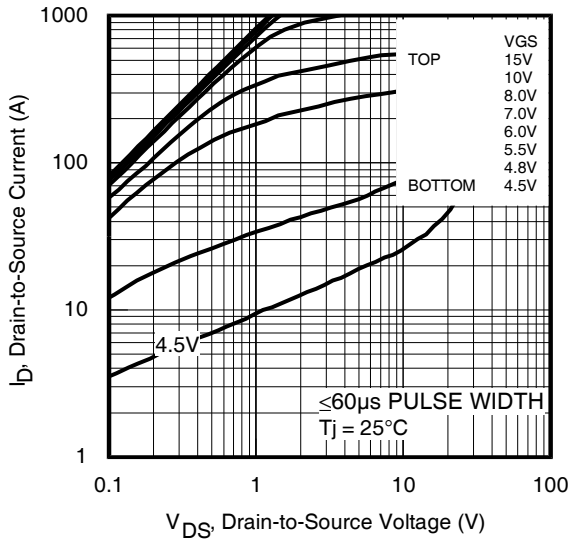


Fig 3. Typical Output Characteristics

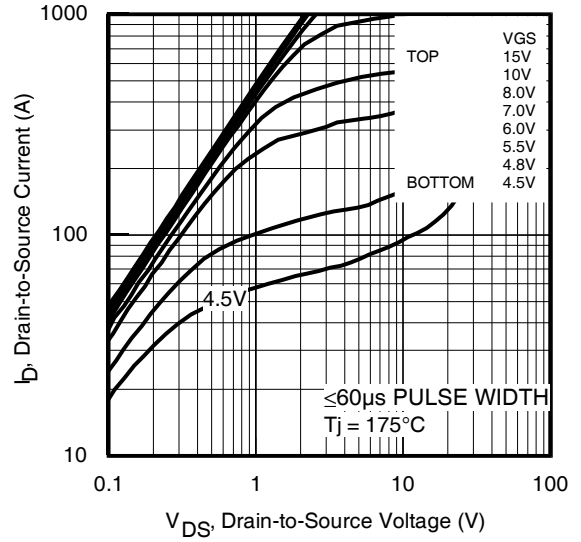


Fig 4. Typical Output Characteristics

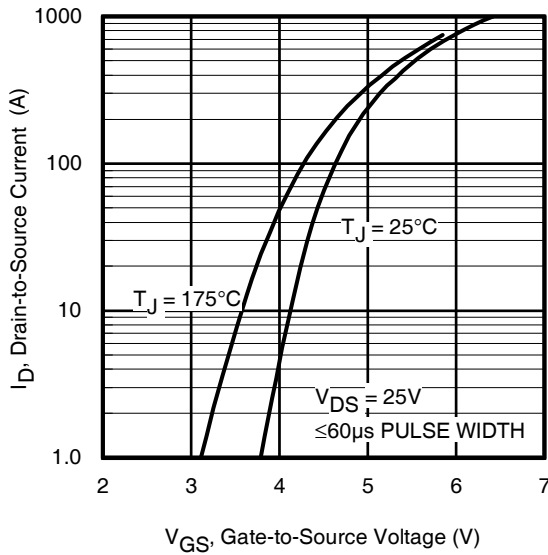


Fig 5. Typical Transfer Characteristics

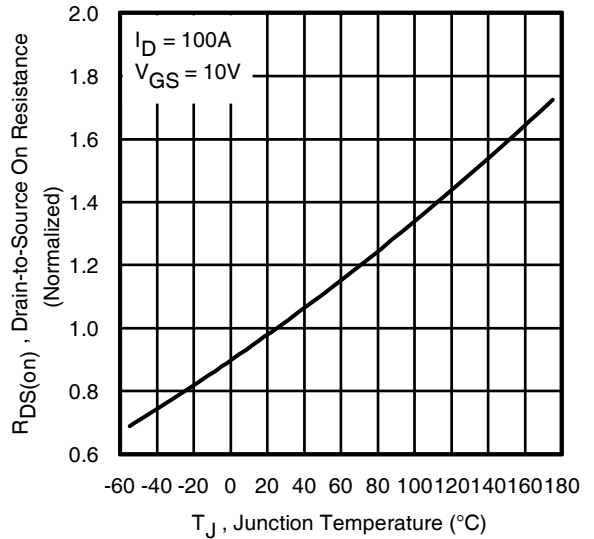


Fig 6. Normalized On-Resistance vs. Temperature

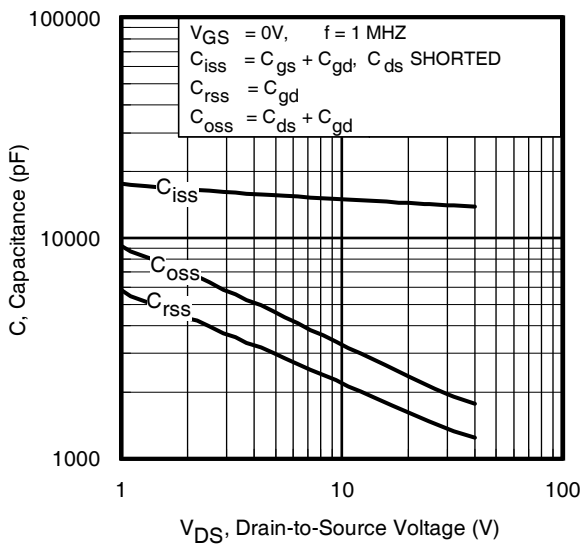


Fig 7. Typical Capacitance vs. Drain-to-Source Voltage

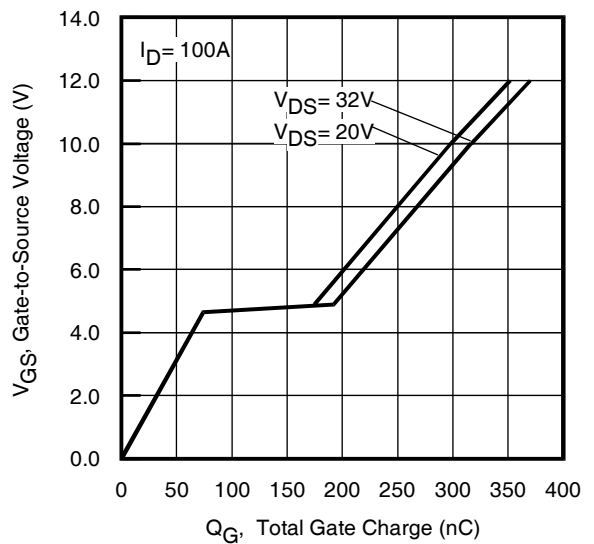
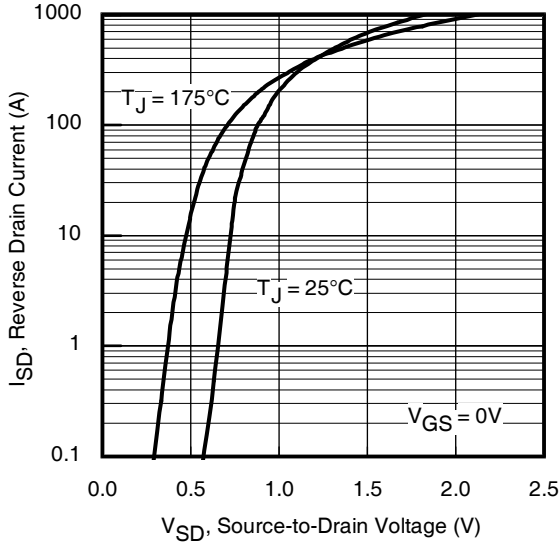
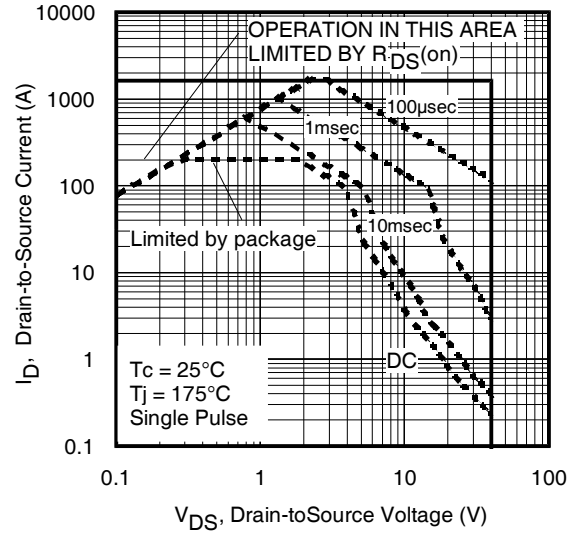


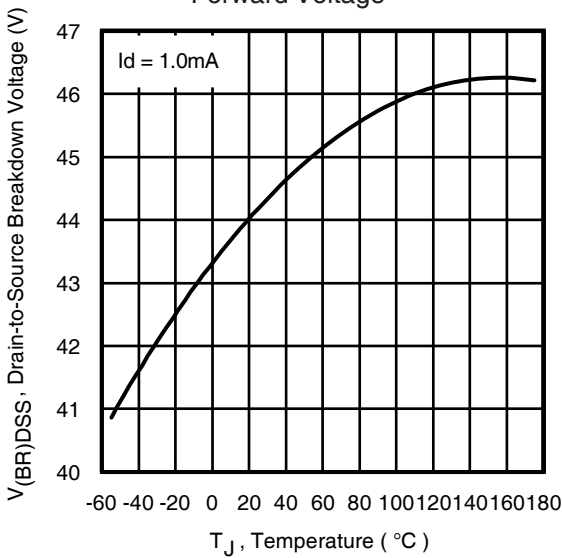
Fig 8. Typical Gate Charge vs. Gate-to-Source Voltage



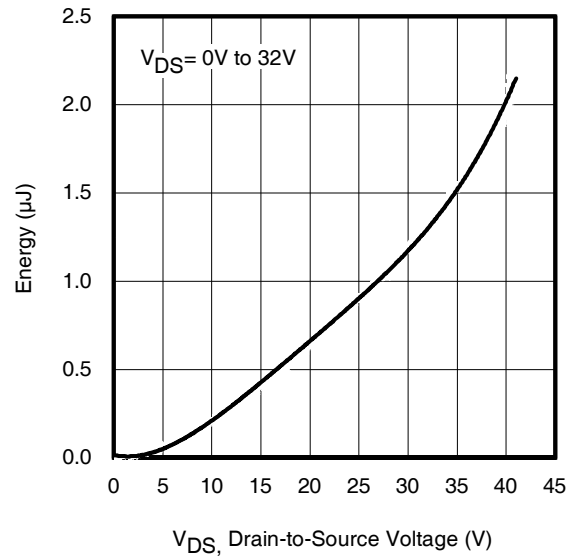
**Fig 9.** Typical Source-Drain Diode Forward Voltage



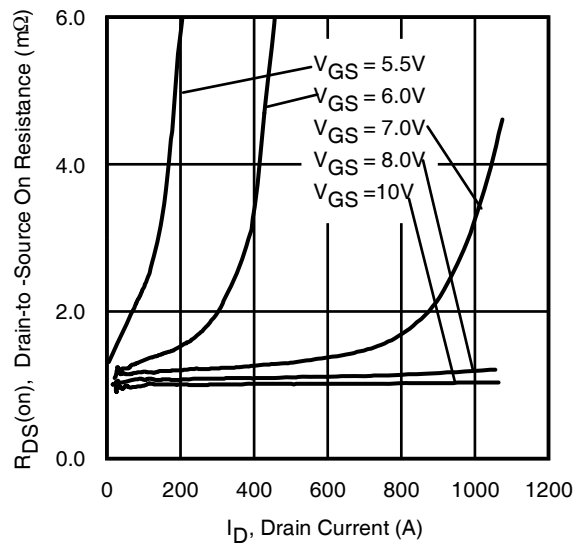
**Fig 10.** Maximum Safe Operating Area



**Fig 11.** Drain-to-Source Breakdown Voltage



**Fig 12.** Typical  $C_{OSS}$  Stored Energy



**Fig 13.** Typical On-Resistance vs. Drain Current

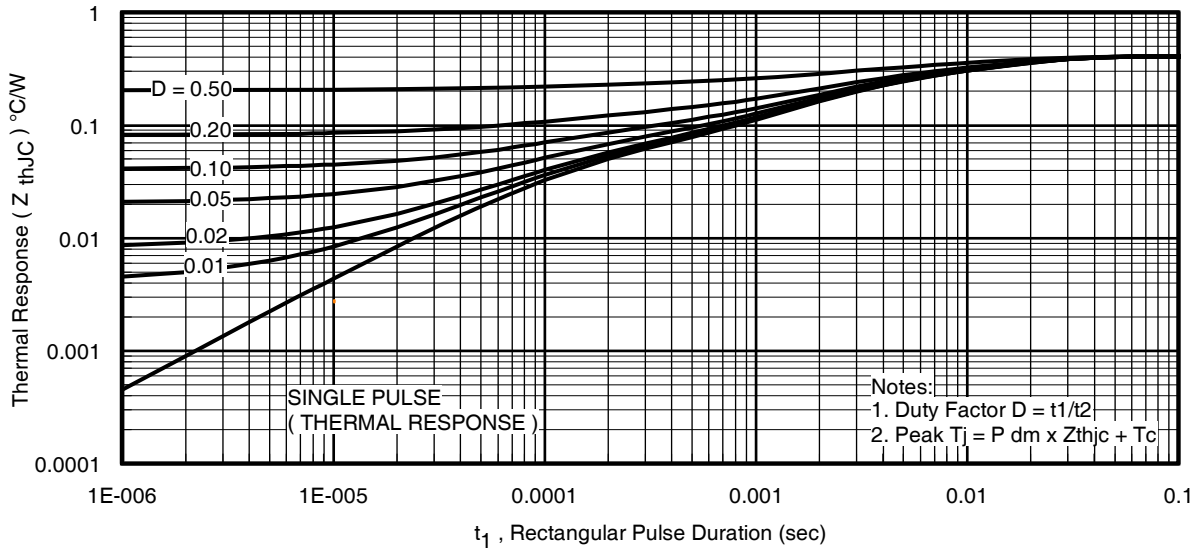


Fig 14. Maximum Effective Transient Thermal Impedance, Junction-to-Case

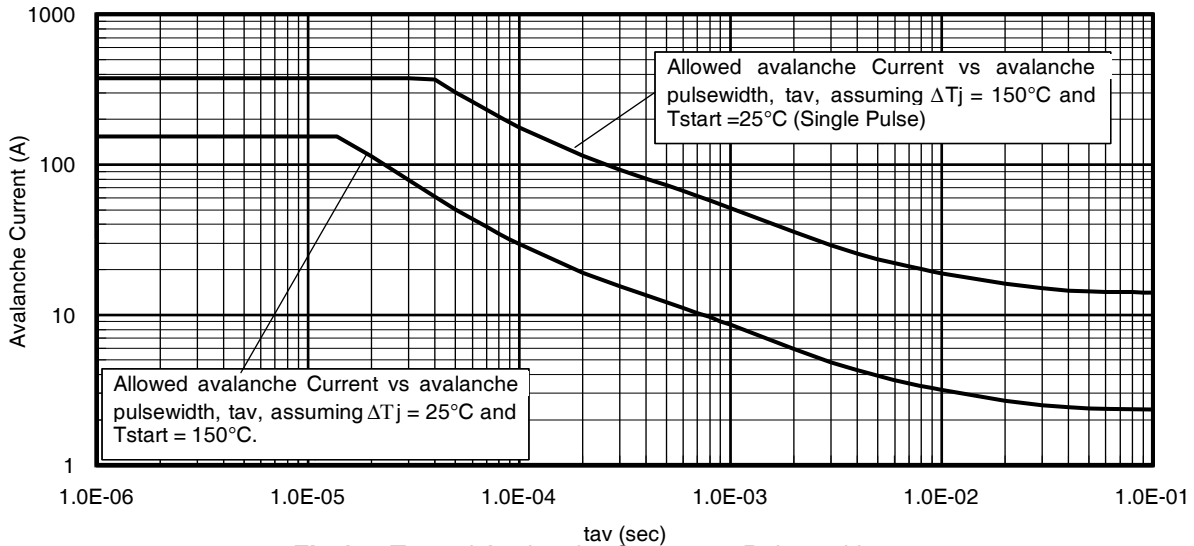


Fig 15. Typical Avalanche Current vs.Pulsewidth

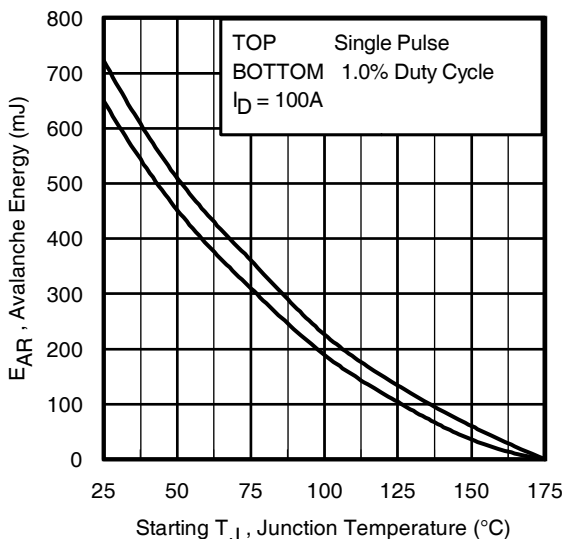


Fig 16. Maximum Avalanche Energy vs. Temperature

**Notes on Repetitive Avalanche Curves , Figures 14, 15:  
(For further info, see AN-1005 at www.irf.com)**

1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5.  $BV$  = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 14, 15).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see Figures 13)

$$P_{D(ave)} = 1/2 ( 1.3 \cdot BV \cdot I_{av} ) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

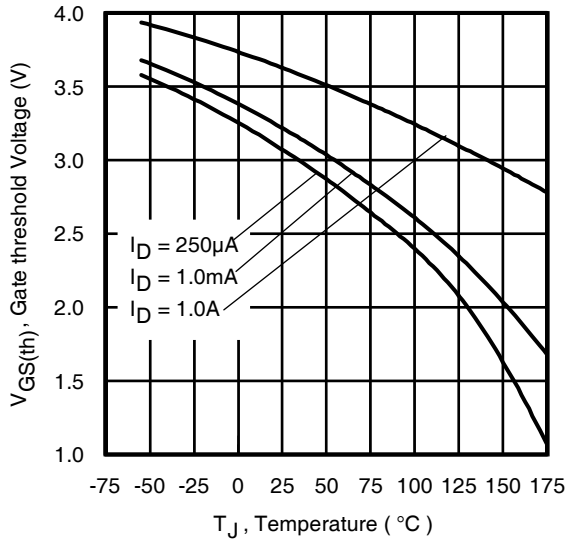


Fig 17. Threshold Voltage vs. Temperature

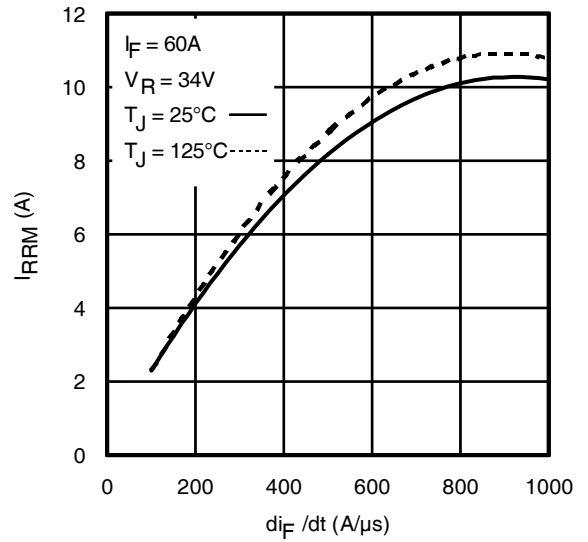


Fig. 18 - Typical Recovery Current vs.  $di_f/dt$

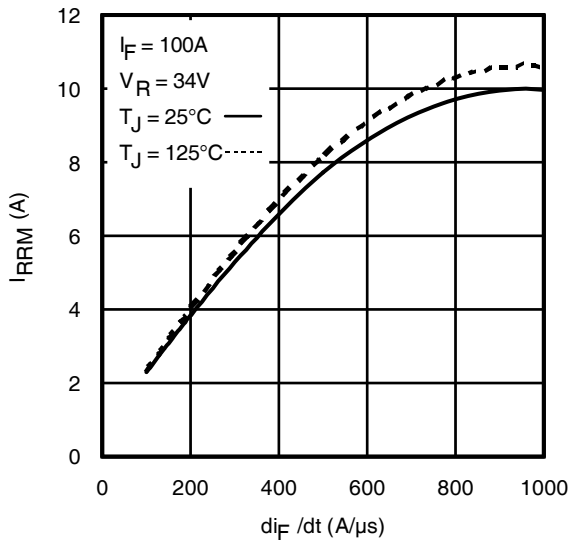


Fig. 19 - Typical Recovery Current vs.  $di_f/dt$

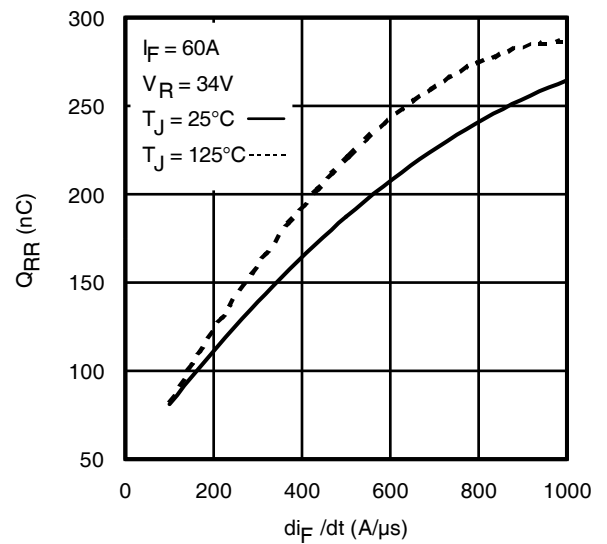


Fig. 20 - Typical Stored Charge vs.  $di_f/dt$

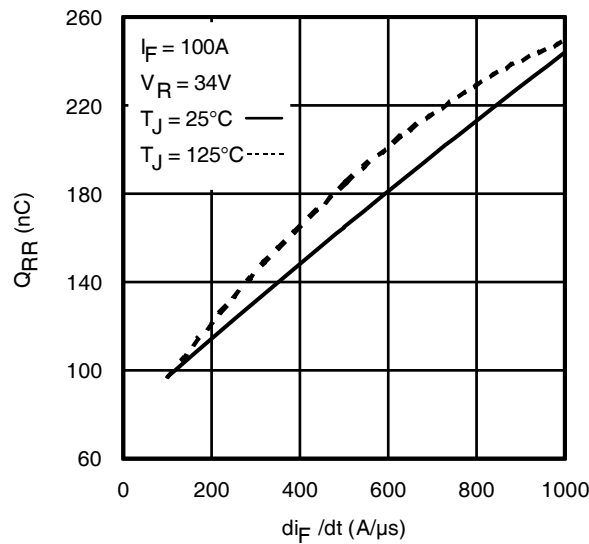
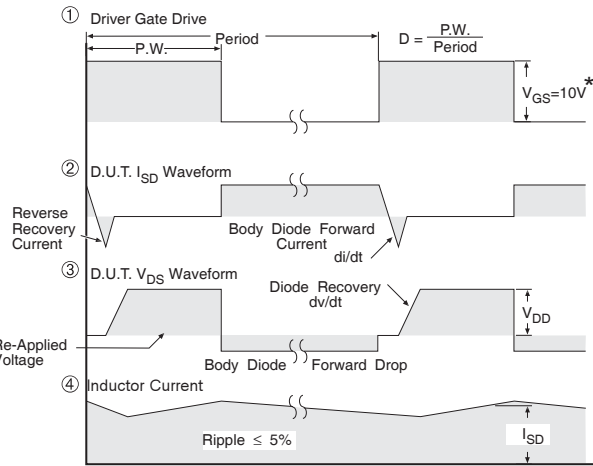
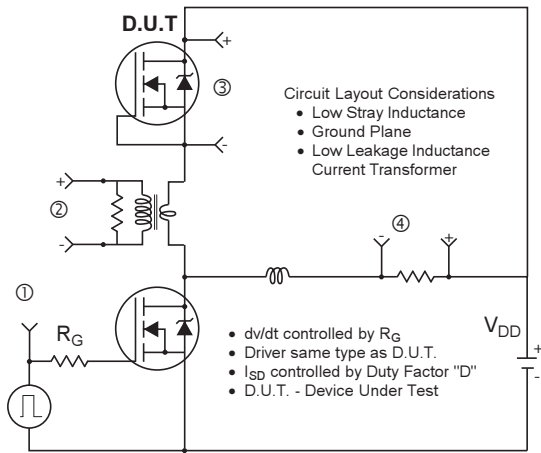
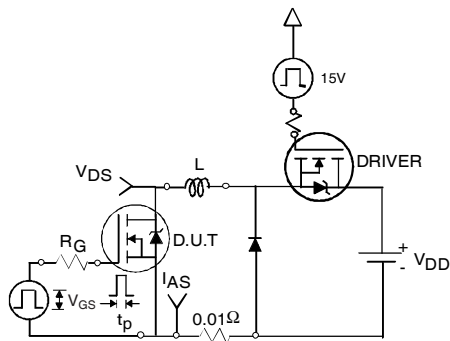


Fig. 21 - Typical Stored Charge vs.  $di_f/dt$

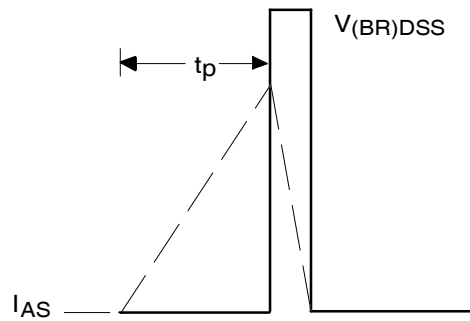


\*  $V_{GS} = 5V$  for Logic Level Devices

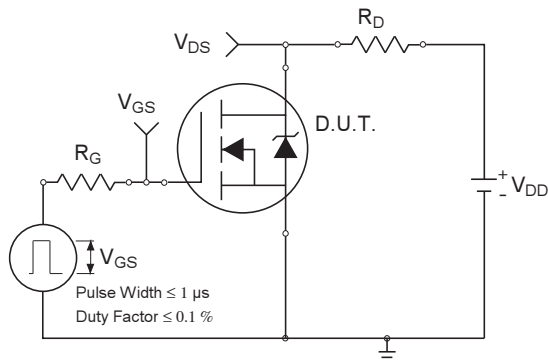
**Fig 22. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs**



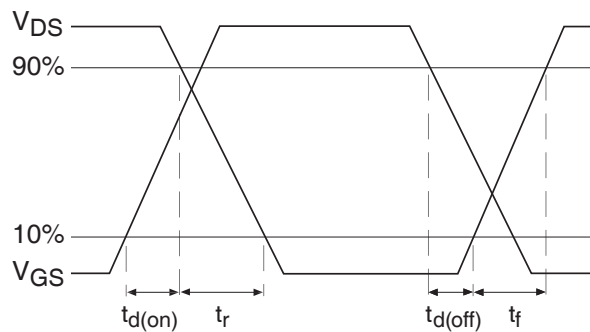
**Fig 22a. Unclamped Inductive Test Circuit**



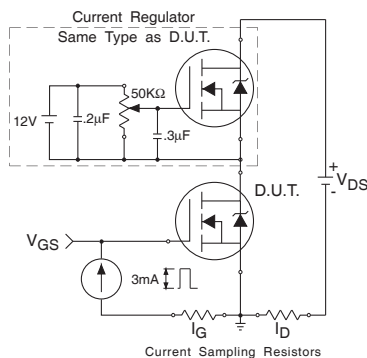
**Fig 22b. Unclamped Inductive Waveforms**



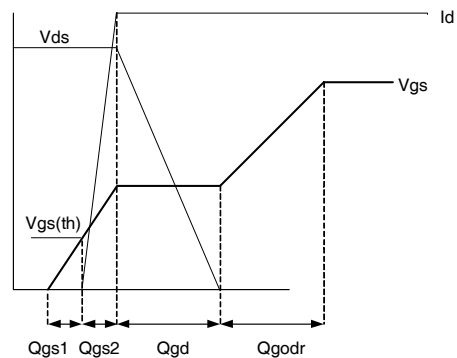
**Fig 23a. Switching Time Test Circuit**



**Fig 23b. Switching Time Waveforms**



**Fig 24a. Gate Charge Test Circuit**

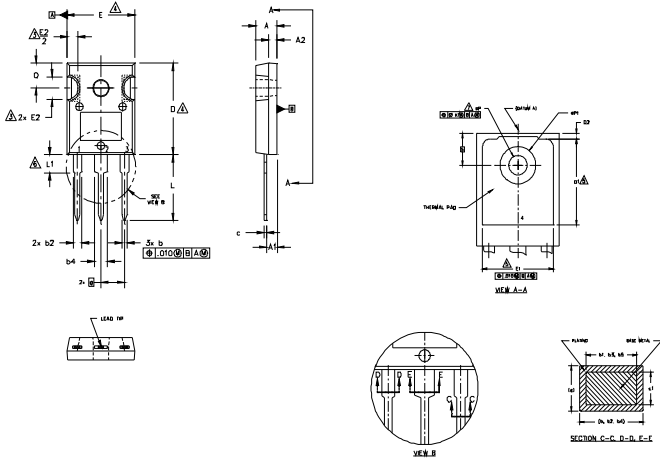


**Fig 24b. Gate Charge Waveform**



## TO-247AC Package Outline

Dimensions are shown in millimeters (inches)



**NOTES:**

1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M 1994.
2. DIMENSIONS ARE SHOWN IN INCHES.
3. CONTOUR OF SLOT OPTIONAL.
4. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS D1 & E1.
6. LEAD FINISH UNCONTROLLED IN L1.
7. ØP TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5 ° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154 INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-247AC .

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	.183	.209	4.65	5.31	
A1	.087	.102	2.21	2.59	
A2	.059	.098	1.50	2.49	
b	.039	.055	0.99	1.40	
b1	.039	.053	0.99	1.35	
b2	.065	.094	1.65	2.39	
b3	.065	.092	1.65	2.34	
b4	.102	.135	2.59	3.43	
b5	.102	.133	2.59	3.38	
c	.015	.035	0.38	0.89	
c1	.015	.033	0.38	0.84	
D	.776	.815	19.71	20.70	4
D1	.515	-	13.08	-	5
D2	.020	.053	0.51	1.35	
E	.602	.625	15.29	15.87	4
E1	.530	-	13.46	-	
E2	.178	.216	4.52	5.49	
Ø	.215 BSC		5.46 BSC		
ØP	.010		0.25		
L	.559	6.34	14.20	16.10	
L1	.146	.169	3.71	4.29	
ØP1	.140	.144	3.56	3.66	
ØP1	-	.291	-	7.39	
O	.209	.224	5.31	5.69	
S	.217 BSC		5.51 BSC		

**LEAD ASSIGNMENTS**

**HEXFET**

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

**IGBTs, CoPACK**

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

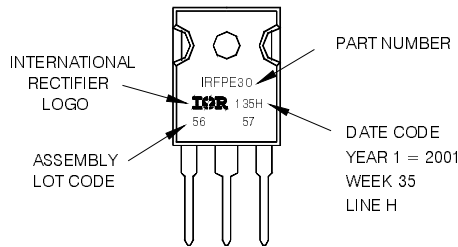
**DIODES**

- 1.- ANODE/OPEN
- 2.- CATHODE
- 3.- ANODE

## TO-247AC Part Marking Information

EXAMPLE: THIS IS AN IRFPE30  
WITH ASSEMBLY  
LOT CODE 5657  
ASSEMBLED ON WW 35, 2001  
IN THE ASSEMBLY LINE 'H'

Note: 'P' in assembly line position  
indicates 'Lead-Free'



TO-247AC package is not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

### Qualification information†

Qualification level	Industrial <sup>††</sup>	
	(per JEDEC JESD47F <sup>†††</sup> guidelines)	
Moisture Sensitivity Level	TO-247AC	N/A (per JEDEC J-STD-020D <sup>†††</sup> )
RoHS compliant	Yes	

† Qualification standards can be found at International Rectifier's web site: <http://www.irf.com/product-info/reliability/>

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information: <http://www.irf.com/whoto-call/salesrep/>

††† Applicable version of JEDEC standard at the time of product release.

Data and specifications subject to change without notice.