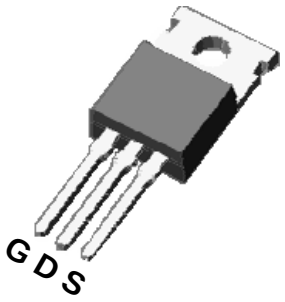
FIR9N90PG

Advanced N-Ch Power MOSFET

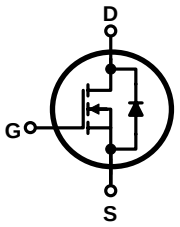
PIN Connection TO-220



Switchng Regulator Application

Features

- Drain-Source breakdown voltage: BV_{DSS}=900V (Min.)
- Low gate charge: Q_g=58nC (Typ.)
- Low drain-source On resistance: $R_{DS(on)}$=1.4Ω (Max.)
- 100% avalanche tested
- RoHS compliant device



Marking Diagram

Y = Year
A = Assembly Location
WW = Work Week
FIR9N90P = Specific Device Code

Absolute maximum ratings (T_C=25°C unless otherwise noted)

Characteristic	Symbol		Rating	Unit
Drain-source voltage	V_{DSS}		900	V
Gate-source voltage	V_{GSS}		±30	V
Drain current (DC) *	I_D	T_c=25°C	9.5	A
		T_c=100°C	6	A
Drain current (Pulsed) *	I_{DM}		38	A
Single pulsed avalanche energy (Note 2)	E_{AS}		860	mJ
Repetitive avalanche current (Note 1)	I_{AR}		9.5	A
Repetitive avalanche energy (Note 1)	E_{AR}		19.8	mJ
Power dissipation	P_D		198	W
Peak diode recovery dv/dt (Note 3)	dv/dt		4.5	V/ns
Junction temperature	T_J		150	°C
Storage temperature range	T_{stg}		-55~150	°C

* Limited only maximum junction temperature

Thermal Characteristics

Characteristic	Symbol	Rating	Unit
Thermal resistance, junction to case	$R_{th(j-c)}$	Max. 0.63	°C/W
Thermal resistance, junction to ambient	$R_{th(j-a)}$	Max. 62.5	

Electrical Characteristics (T_C=25°C unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Drain-source breakdown voltage	BV_{DSS}	I_D=250uA, V_{GS}=0	900	-	-	V
Gate threshold voltage	$V_{GS(th)}$	I_D=250uA, V_{DS}=V_{GS}	2	-	4	V
Drain-source cut-off current	I_{DSS}	V_{DS}=900V, V_{GS}=0V	-	-	10	uA
		V_{DS}=720V, T_c=125°C	-	-	100	uA
Gate leakage current	I_{GSS}	V_{DS}=0V, V_{GS}=±30V	-	-	±100	nA
Drain-source on-resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=4.75A	-	1.13	1.4	Ω
Forward transfer conductance (Note 4)	g_{fs}	V_{DS}=10V, I_D=4.75A	-	10	-	S
Input capacitance	C_{iss}	V_{DS}=25V, V_{GS}=0V, f=1.0MHz	-	2548	3440	pF
Output capacitance	C_{oss}		-	197	266	
Reverse transfer capacitance	C_{rss}		-	32	51	
Turn-on delay time (Note 4,5)	$t_{d(on)}$	V_{DD}=450V, I_D=9.5A, R_G=25Ω	-	61	-	ns
Rise time (Note 4,5)	t_r		-	49	-	
Turn-off delay time (Note 4,5)	$t_{d(off)}$		-	318	-	
Fall time (Note 4,5)	t_f		-	100	-	
Total gate charge (Note 4,5)	Q_g	V_{DS}=720V, V_{GS}=10V, I_D=9.5A	-	58	78	nC
Gate-source charge (Note 4,5)	Q_{gs}		-	11	-	
Gate-drain charge (Note 4,5)	Q_{gd}		-	22	-	

Source-Drain Diode Ratings and Characteristics (T_C=25°C unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Source current (DC)	I_S	Integral reverse diode in the MOSFET	-	-	9.5	A
Source current (Pulsed)	I_{SM}		-	-	38	A
Forward voltage	V_{SD}	V_{GS}=0V, I_S=9.5A	-	-	1.5	V
Reverse recovery time (Note 4,5)	t_{rr}	I_S=9.5A, V_{GS}=0V dI_F/dt=100A/us	-	550	-	ns
Reverse recovery charge (Note 4,5)	Q_{rr}		-	6.5	-	uC

Note:
1. Repeated rating: Pulse width limited by safe operating area
2. L=18mH, I_{AS}=9.5A, V_{DD}=50V, R_G=25Ω, Starting T_J=25°C
3. I_{SD}≤9A, di/dt≤200A/us, V_{DD}≤BV_{DSS}, Starting T_J=25°C
4. Pulse test: Pulse width≤300us, Duty cycle≤2%
5. Essentially independent of operating temperature typical characteristics

Electrical Characteristics Curve

Fig. 1 I_D - V_{DS}

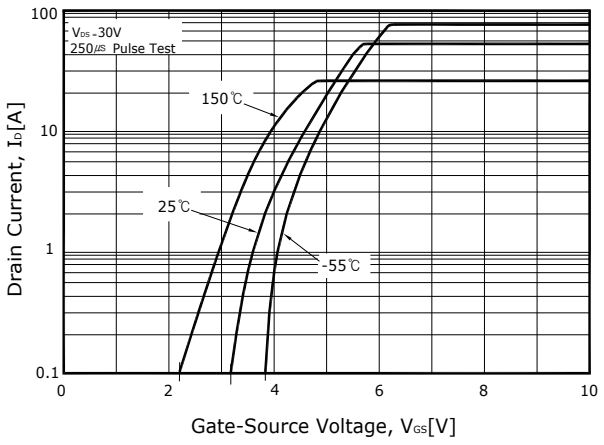


Fig. 2 I_D - V_{GS}

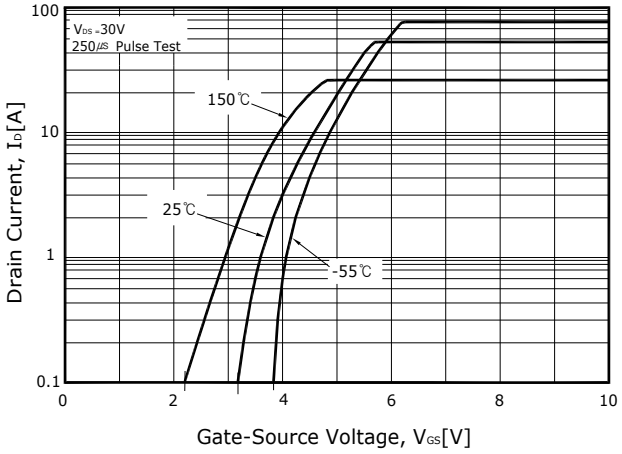


Fig. 3 $R_{DS(ON)}$ - I_D

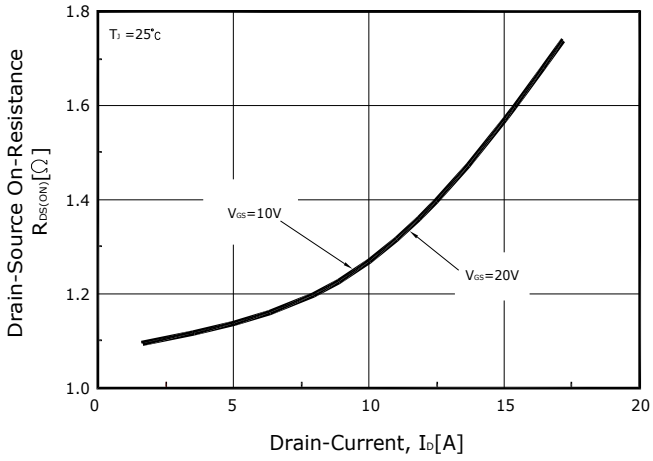


Fig. 4 I_{DR} - V_{SD}

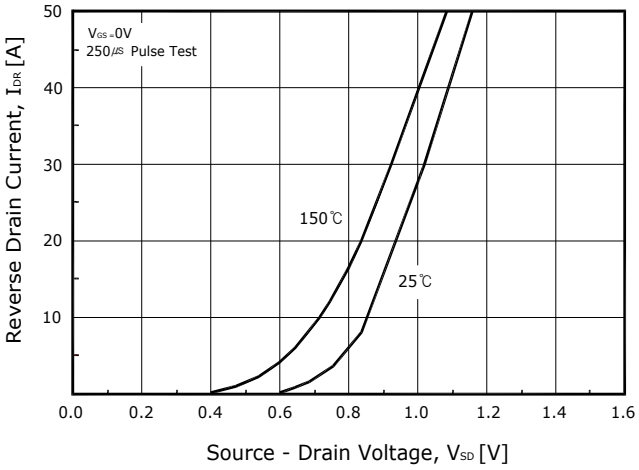


Fig. 5 Capacitance - V_{DS}

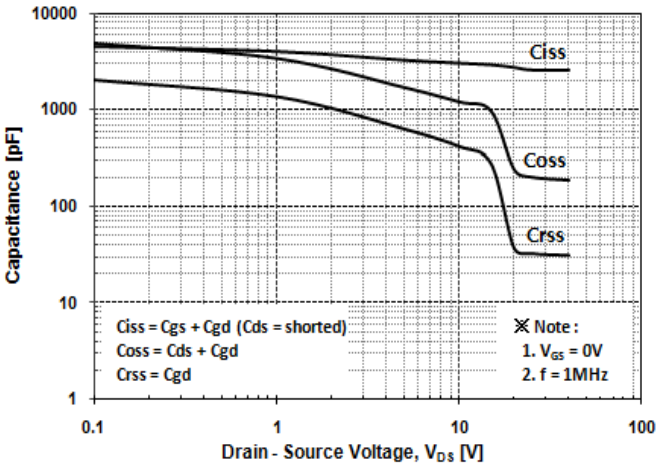
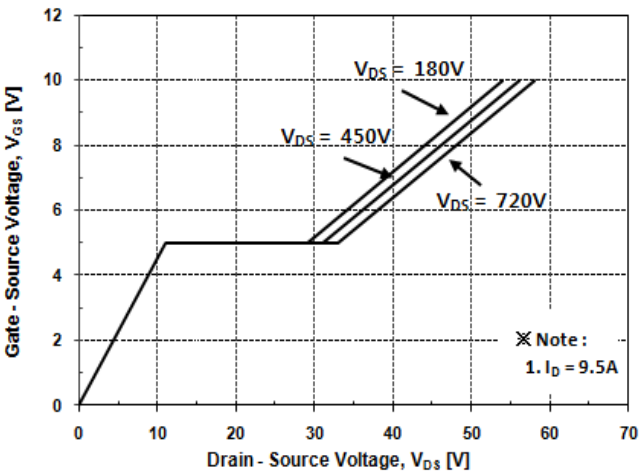


Fig. 6 V_{GS} - Q_G



Electrical Characteristics Curve (Continue)

Fig. 7 BV_{DSS} - T_J

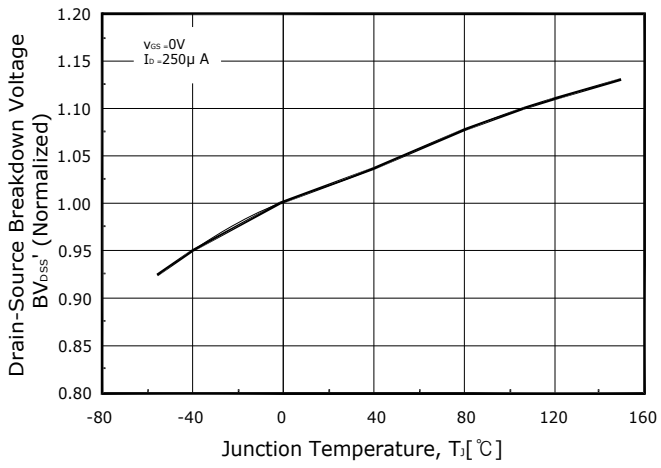


Fig. 8 $R_{DS(ON)}$ - T_J

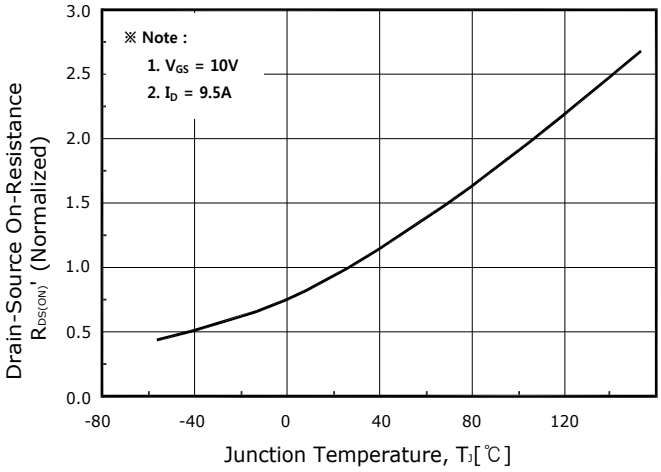


Fig. 9 I_D - T_C

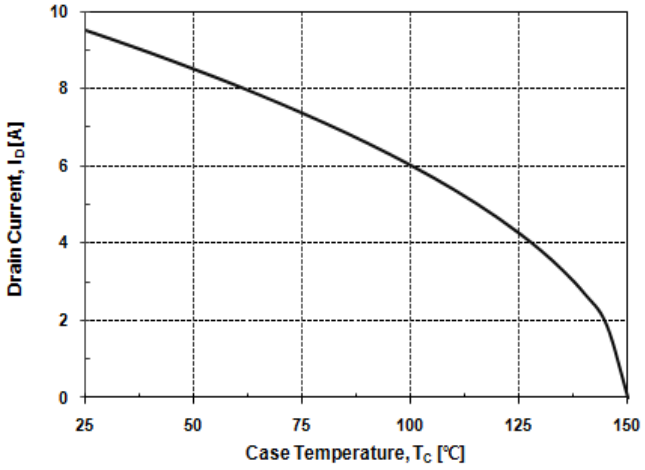


Fig. 10 Safe Operating Area

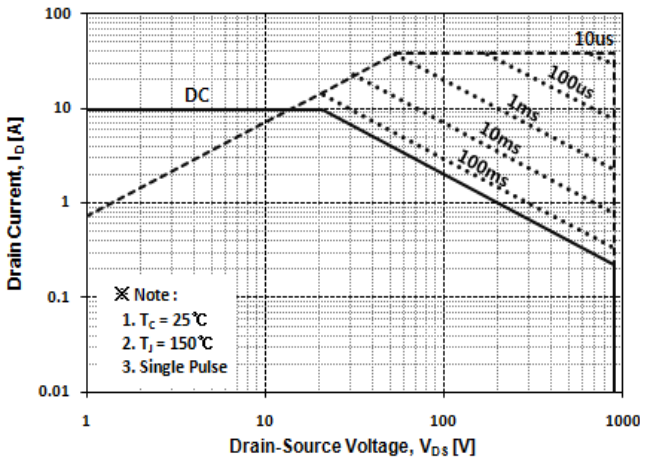


Fig. 11 Transient Thermal Impedance

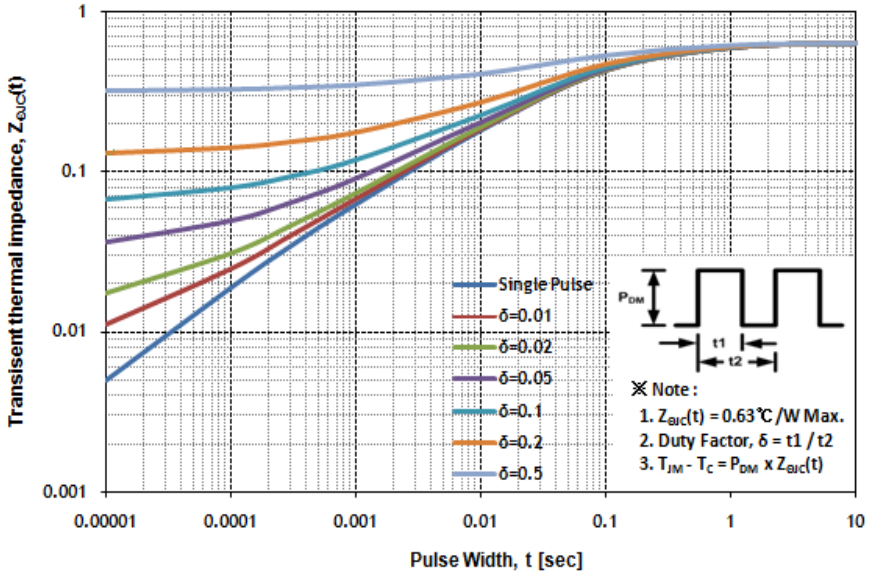
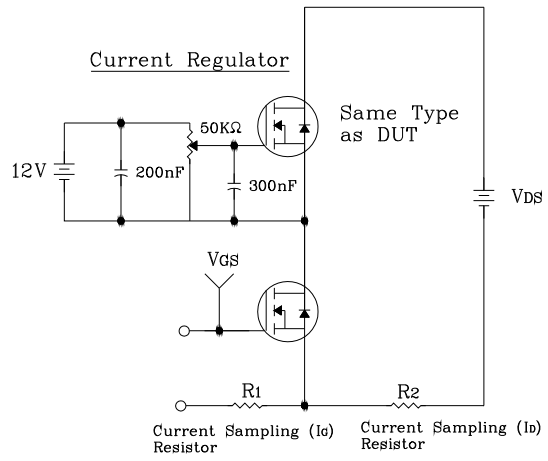


Fig. 12 Gate Charge Test Circuit & Waveform



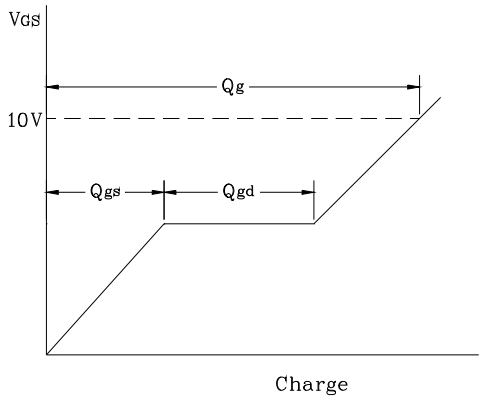
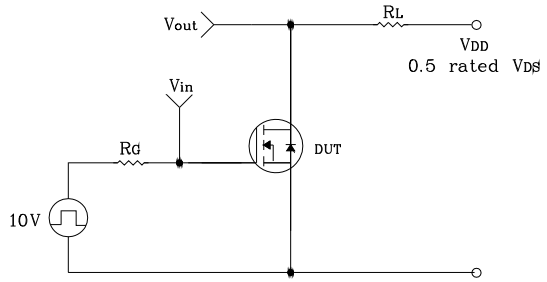


Fig. 13 Resistive Switching Test Circuit & Waveform



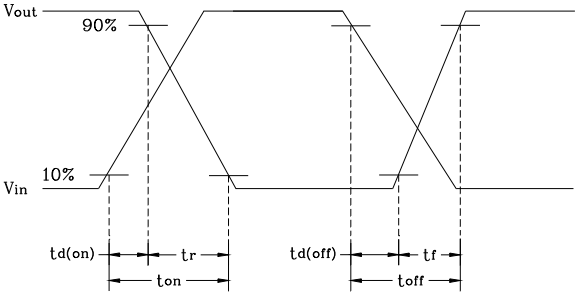
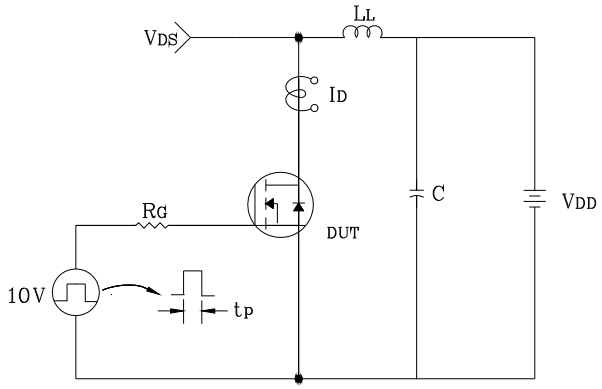


Fig. 14 E_{AS} Test Circuit & Waveform



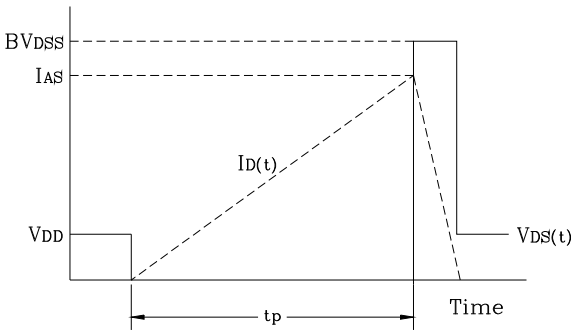
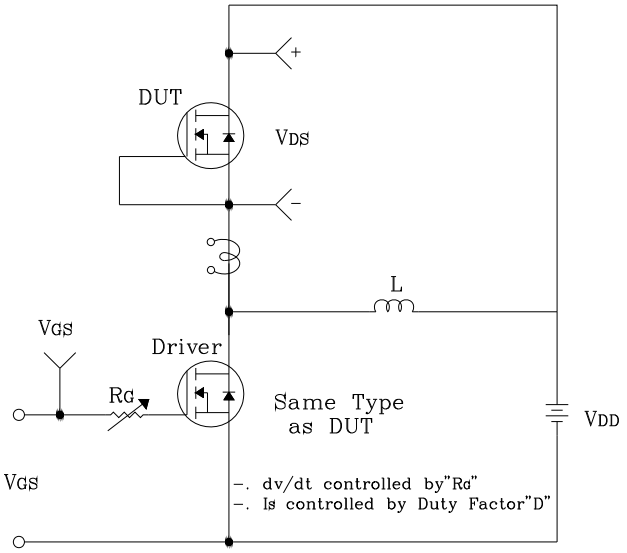
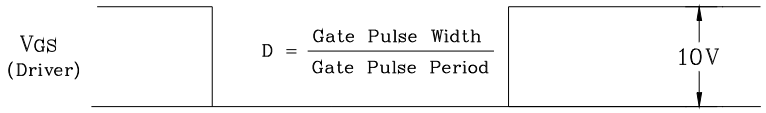
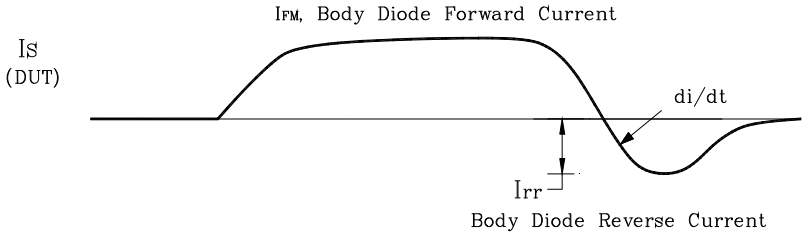
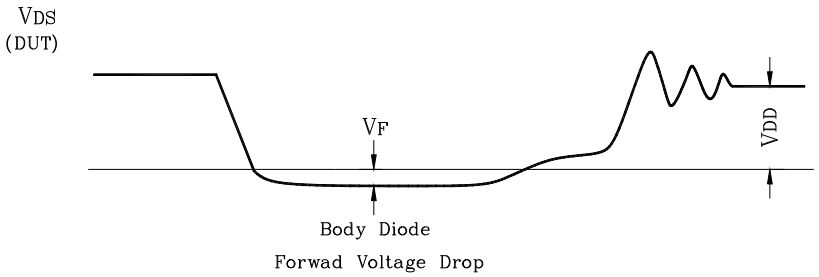


Fig. 15 Diode Reverse Recovery Time Test Circuit & Waveform



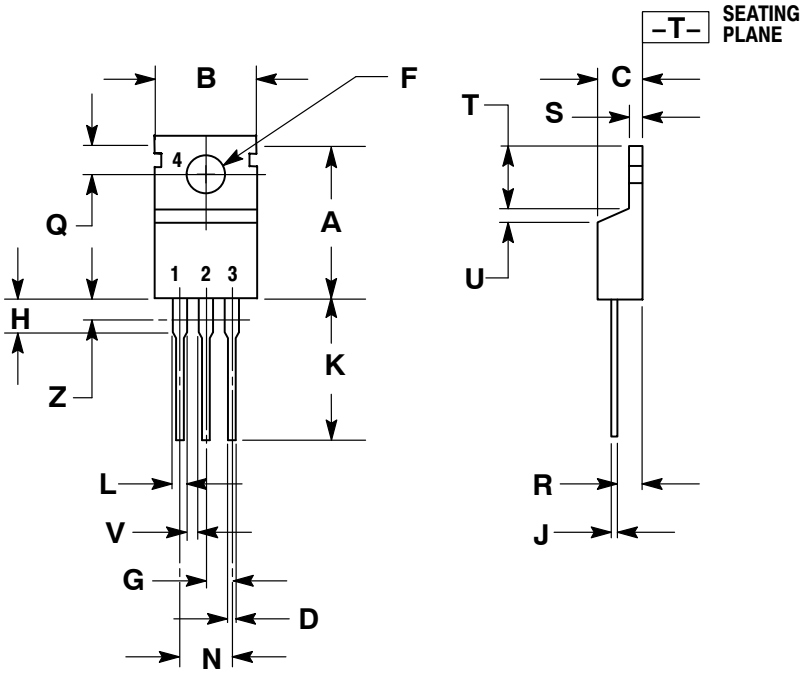






Package Dimensions

TO-220



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.161	3.61	4.09
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.014	0.025	0.36	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 6:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE