Complementary Power Transistors

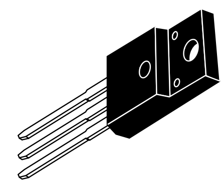
For Isolated Package Applications

NPN
MJF15030
PNP
MJF15031

Designed for general–purpose amplifier and switching applications, where the mounting surface of the device is required to be electrically isolated from the heatsink or chassis.

- Electrically Similar to the Popular MJE15030 and MJE15031
- 150 $V_{CEO(sus)}$
- 8 A Rated Collector Current
- No Isolating Washers Required
- Reduced System Cost
- High Current Gain–Bandwidth Product
  f_T = 30 MHz (Min) @ I_C = 500 mAdc
- UL Recognized, File #E69369, to 3500 V_{RMS} Isolation

**COMPLEMENTARY
SILICON
POWER TRANSISTORS
8 AMPERES
150 VOLTS
36 WATTS**



**CASE 221D–02
TO–220 TYPE**

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Collector–Emitter Voltage		V_{CEO}	150	Vdc
Collector–Base Voltage		V_{CB}	150	Vdc
Emitter–Base Voltage		V_{EB}	5	Vdc
RMS Isolation Voltage (1) (for 1 sec, R.H. < 30%, T_A = 25°C)	Test No. 1 Per Fig. 11 Test No. 2 Per Fig. 12 Test No. 3 Per Fig. 13	V_{ISOL}	4500 3500 1500	V_{RMS}
Collector Current — Continuous — Peak		I_C	8 16	Adc
Base Current		I_B	2	Adc
Total Power Dissipation* @ T_C = 25°C Derate above 25°C		P_D	36 0.29	Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C		P_D	2 0.016	Watts W/°C
Operating and Storage Junction Temperature Range		T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction to Case*	$R_{\theta JC}$	3.5	°C/W
Lead Temperature for Soldering Purpose	T_L	260	°C

* Measurement made with thermocouple contacting the bottom insulated mounting surface (in a location beneath the die), the device mounted on a heatsink with thermal grease and a mounting torque of ≥ 6 in. lbs.
(1) Proper strike and creepage distance must be provided.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (1) (I_C = 10 mAdc, I_B = 0)	$V_{CEO(sus)}$	150	—	Vdc
Collector Cutoff Current (V_{CE} = 150 Vdc, I_B = 0)	I_{CEO}	—	10	μAdc
Collector Cutoff Current (V_{CB} = 150 Vdc, I_E = 0)	I_{CBO}	—	10	μAdc
Emitter Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)	I_{EBO}	—	10	μAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 0.1 Adc, V_{CE} = 2 Vdc) (I_C = 2 Adc, V_{CE} = 2 Vdc) (I_C = 3 Adc, V_{CE} = 2 Vdc) (I_C = 4 Adc, V_{CE} = 2 Vdc)	h_{FE}	40 40 40 20	— — — —	—
DC Current Gain Linearity (V_{CE} from 2 V to 20 V, I_C from 0.1 A to 3 A) (NPN to PNP)	h_{FE}	Typ 2 3		
Collector–Emitter Saturation Voltage (I_C = 1 Adc, I_B = 0.1 Adc)	$V_{CE(sat)}$	—	0.5	Vdc
Base–Emitter On Voltage (I_C = 1 Adc, V_{CE} = 2 Vdc)	$V_{BE(on)}$	—	1	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain–Bandwidth Product (2) (I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)	f_T	30	—	MHz

NOTES:
1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. $f_T = |h_{fe}| \bullet f_{test}$.

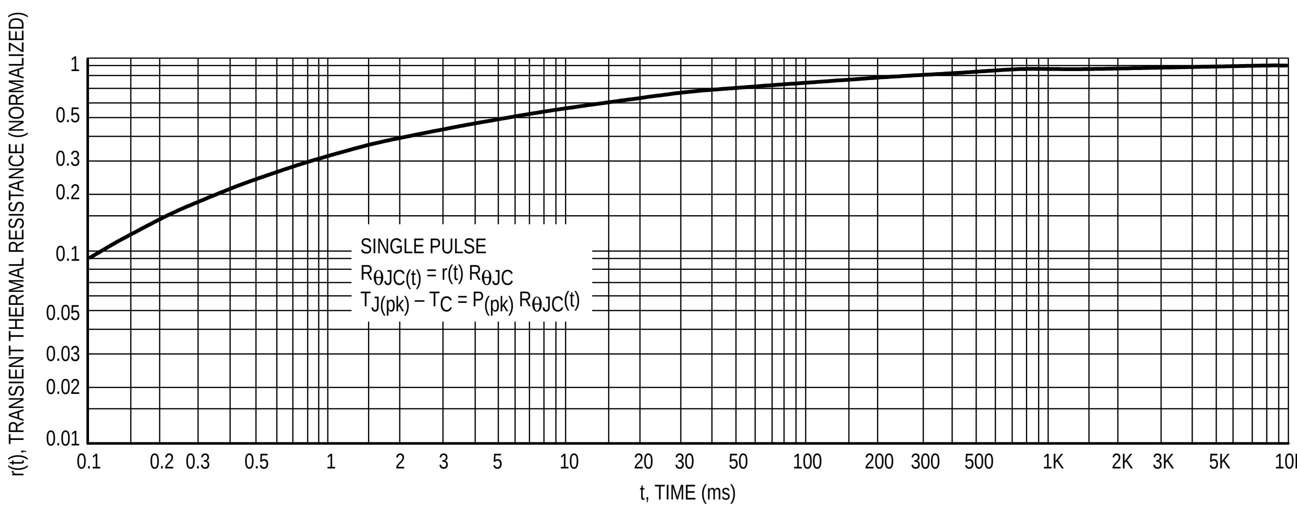


Figure 1. Thermal Response

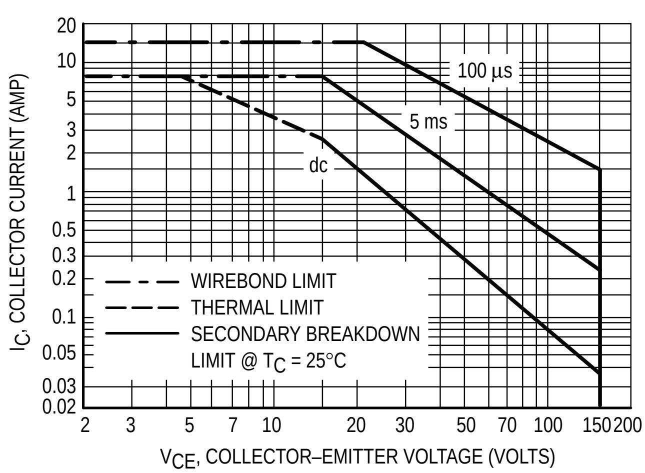


Figure 2. Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C – V_{CE} limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 2 and 3 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ < 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 1. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

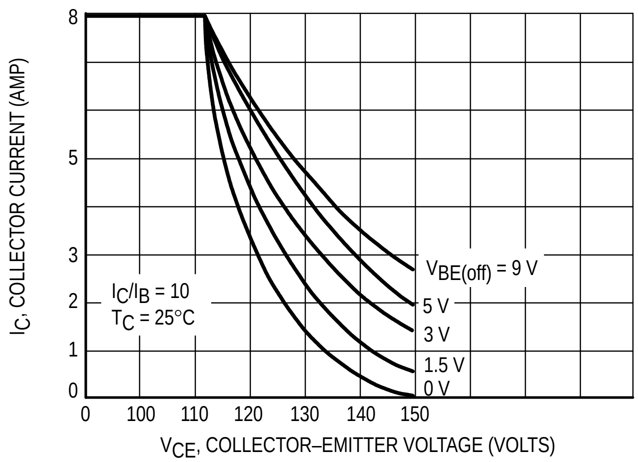


Figure 3. Reverse Bias Switching Safe Operating Area

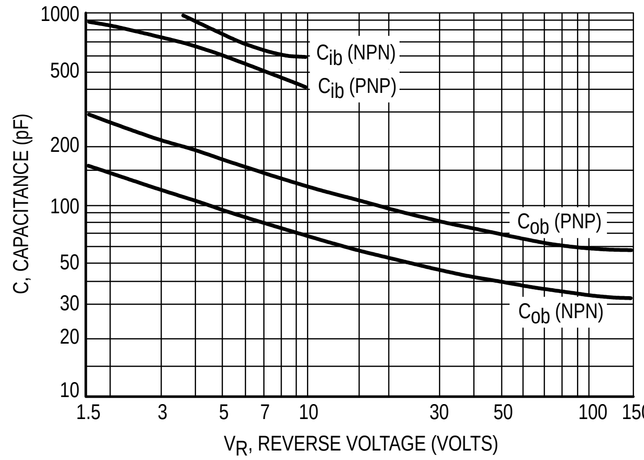


Figure 4. Capacitances

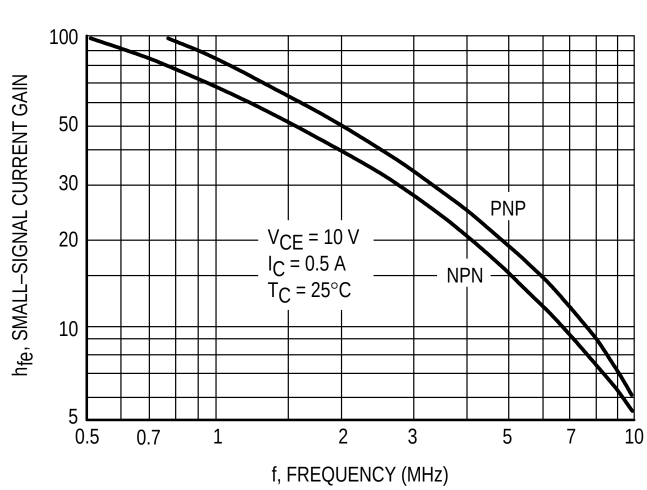


Figure 5. Small–Signal Current Gain

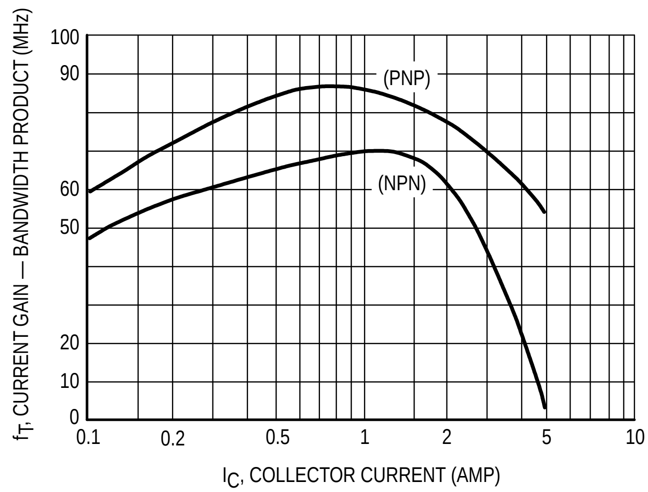


Figure 6. Current Gain — Bandwidth Product

DC CURRENT GAIN

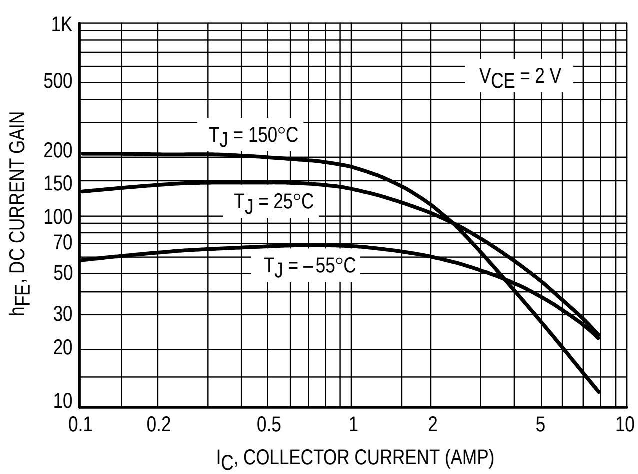


Figure 7a. MJF15030 NPN

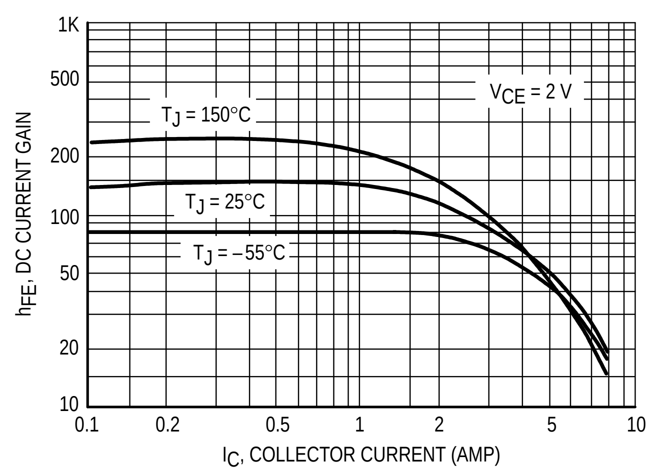


Figure 7b. MJF15031 PNP

"ON" VOLTAGE

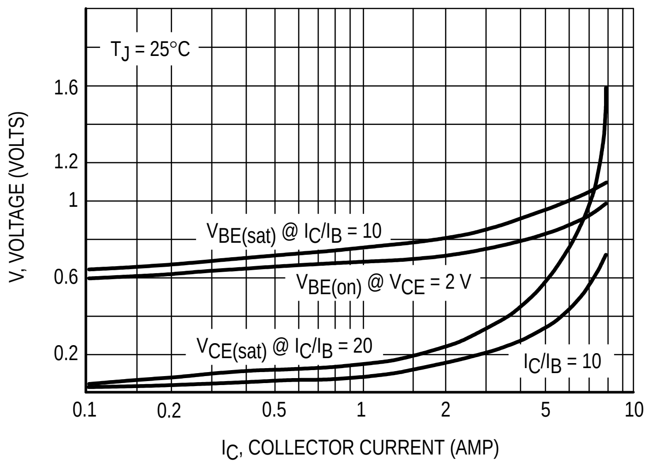


Figure 8a. MJF15030 NPN

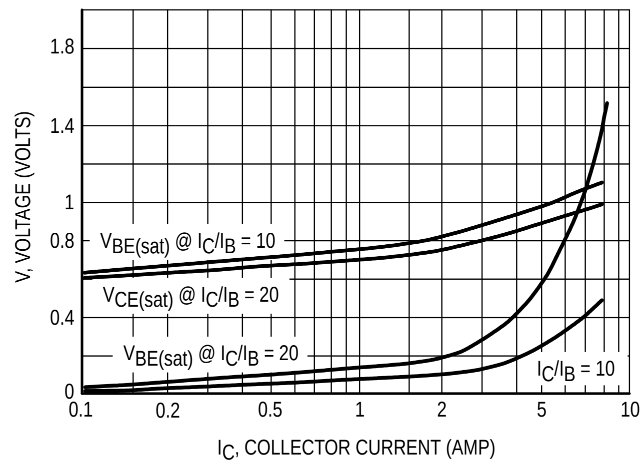


Figure 8b. MJF15031 PNP

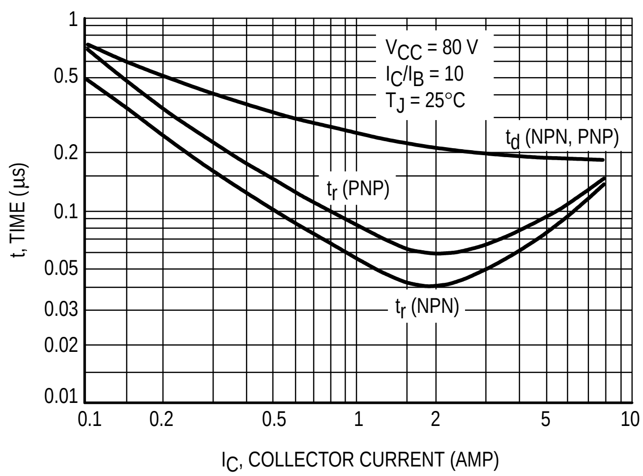


Figure 9. Turn–On Times

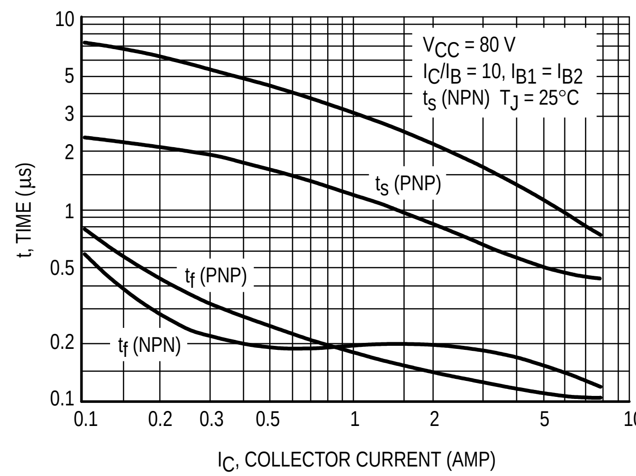


Figure 10. Turn–Off Times

TEST CONDITIONS FOR ISOLATION TESTS*

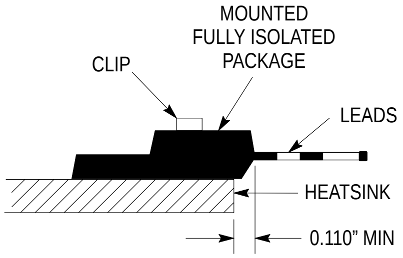


Figure 11. Clip Mounting Position for Isolation Test Number 1

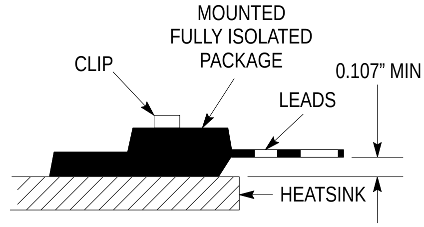


Figure 12. Clip Mounting Position for Isolation Test Number 2

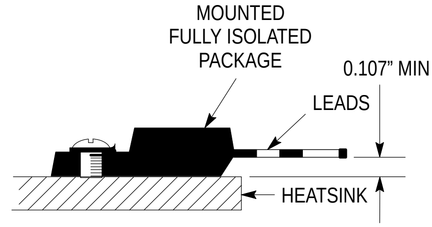


Figure 13. Screw Mounting Position for Isolation Test Number 3

* Measurement made between leads and heatsink with all leads shorted together

MOUNTING INFORMATION

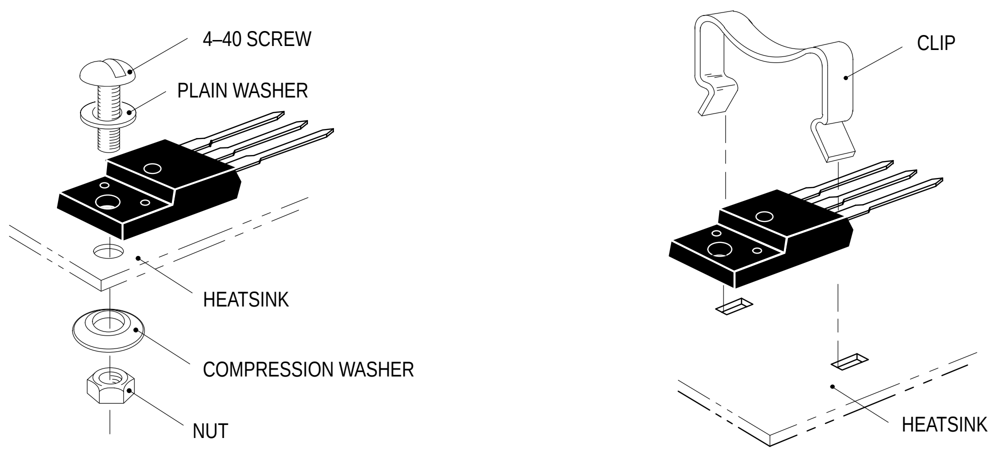


Figure 14. Typical Mounting Techniques*

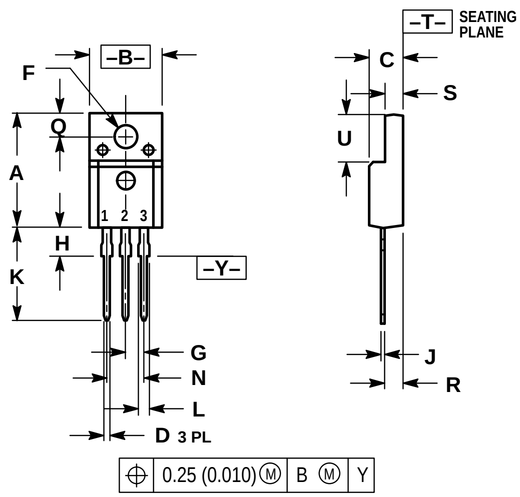
Laboratory tests on a limited number of samples indicate, when using the screw and compression washer mounting technique, a screw torque of 6 to 8 in · lbs is sufficient to provide maximum power dissipation capability. The compression washer helps to maintain a constant pressure on the package over time and during large temperature excursions.

Destructive laboratory tests show that using a hex head 4–40 screw, without washers, and applying a torque in excess of 20 in · lbs will cause the plastic to crack around the mounting hole, resulting in a loss of isolation capability.

Additional tests on slotted 4–40 screws indicate that the screw slot fails between 15 to 20 in · lbs without adversely affecting the package. However, in order to positively ensure the package integrity of the fully isolated device, Motorola does not recommend exceeding 10 in · lbs of mounting torque under any mounting conditions.

** For more information about mounting power semiconductors see Application Note AN1040.

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.621	0.629	15.78	15.97
B	0.394	0.402	10.01	10.21
C	0.181	0.189	4.60	4.80
D	0.026	0.034	0.67	0.86
F	0.121	0.129	3.08	3.27
G	0.100 BSC		2.54 BSC	
H	0.123	0.129	3.13	3.27
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.14	1.52
N	0.200 BSC		5.08 BSC	
Q	0.126	0.134	3.21	3.40
R	0.107	0.111	2.72	2.81
S	0.096	0.104	2.44	2.64
U	0.259	0.267	6.58	6.78

STYLE 2:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

CASE 221D–02
TO–220 TYPE
ISSUE D

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