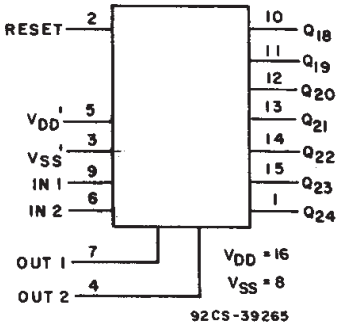
TEXAS INSTRUMENTS
Data sheet acquired from Harris Semiconductor
SCHS078C -- Revised October 2003

CD4521B Types

CMOS 24-Stage Frequency Divider

High-Voltage Types (20-Volt Rating)



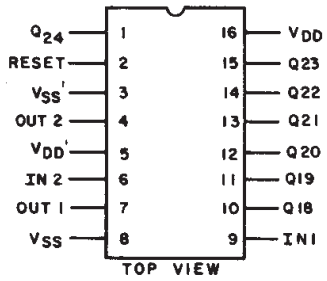
FUNCTIONAL DIAGRAM

Features:

- *Reset disables the RC oscillator for low-power standby condition*
- *V_{DD}' and V_{SS}' pins are brought out from the crystal oscillator to allow use of external resistors for low-power operation*
- *Maximum input current of 1 μA at 18 V over full package-temperature range: 100 nA at 18 V and 25°C*
- *Common reset*
- *100% tested for 20-V quiescent current*
- *5, 10 and 15 V parametric ratings*
- *Standardized symmetrical output characteristics*
- *Meets all requirements of JEDEC Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"*

■ CD4521B consists of an oscillator section and 24 ripple-carry binary counter stages. The oscillator configuration (using IN1) allows design of either RC or crystal oscillator circuits. IN1 should be tied either HIGH or LOW when not in use. A HIGH on the RESET causes the counter to go to the all-0's state and disables the oscillator. The count is advanced on the negative transition of IN1 (and IN2). A time-saving test mode is described in the Functional Test Sequence Table and in Fig. 6.

The CD4521B types are supplied in 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (M, M96, MT, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).



TERMINAL ASSIGNMENT

OUTPUT	COUNT CAPACITY
Q18	2^{18} = 262,144
Q19	2^{19} = 524,288
Q20	2^{20} = 1,048,576
Q21	2^{21} = 2,097,152
Q22	2^{22} = 4,194,304
Q23	2^{23} = 8,388,608
Q24	2^{24} = 16,777,216

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) ..... -0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5V to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55°C to +100°C 500mW
For T_A = +100°C to +125°C ..... Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55°C to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max ..... +265°C

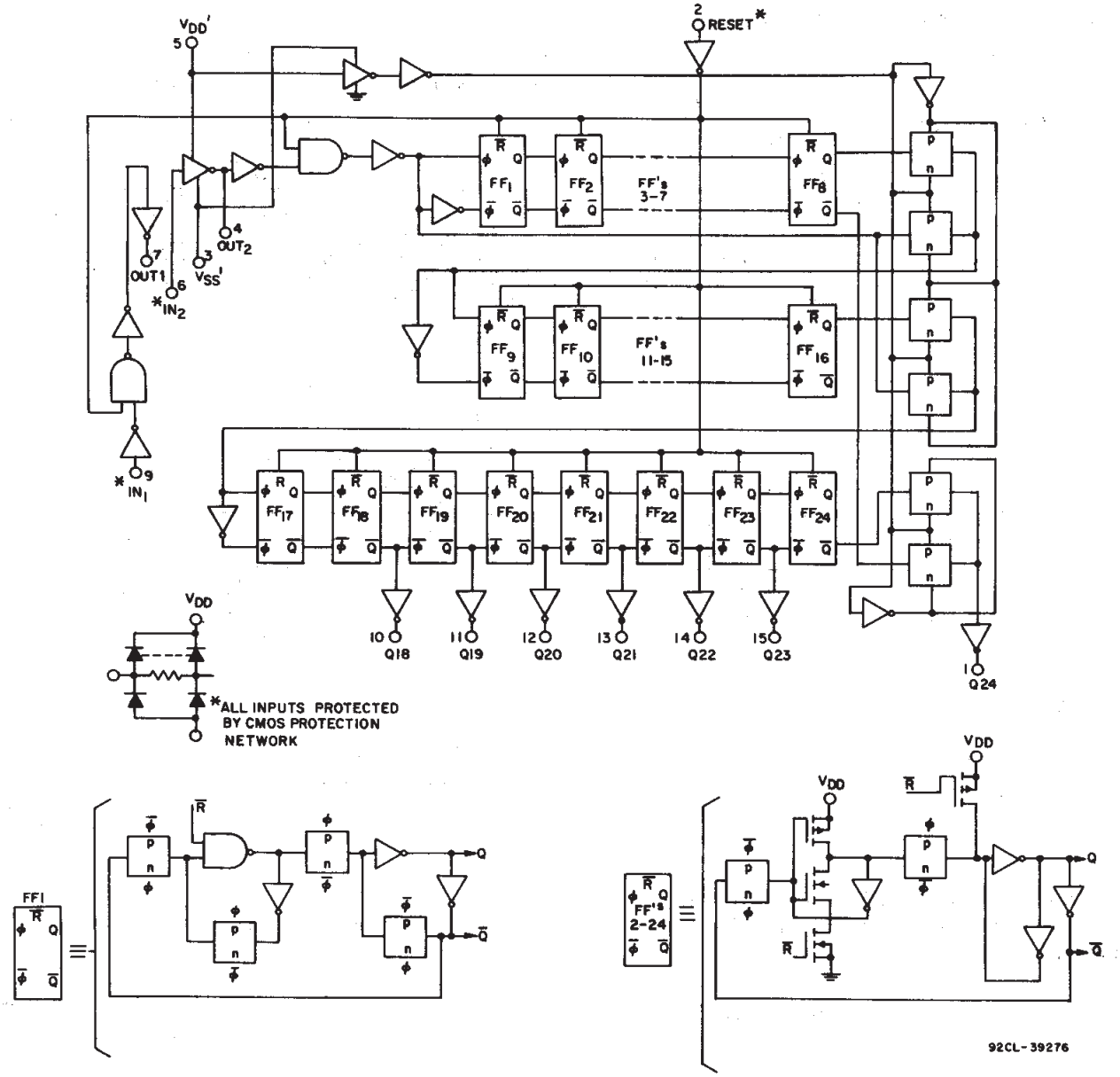


Fig. 1 - Logic diagram for CD4521B.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	-40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current, I_{DD} Max.	—	0, 5	5	5	5	150	150	—	0.04	5	μA
	—	0, 10	10	10	10	300	300	—	0.04	10	
	—	0, 15	15	20	20	600	600	—	0.04	20	
	—	0, 20	20	100	100	3000	3000	—	0.08	100	
Output Low (Sink) Current, I_{OL} Min.	0.4	0, 5	5	0.64	0.61	0.42	0.36	0.51	1	—	mA
	0.5	0, 10	10	1.6	1.5	1.1	0.9	1.3	2.6	—	
	1.5	0, 15	15	4.2	4	2.8	2.4	3.4	6.8	—	
Output High (Source) Current, I_{OH} Min.	4.6	0, 5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	—	
	2.5	0, 5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	—	
	9.5	0, 10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	—	
	13.5	0, 15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	—	
Output Voltage: Low-Level, V_{OL} Max.	—	0, 5	5	0.05				—	0	0.05	V
	—	0, 10	10	0.05				—	0	0.05	
	—	0, 15	15	0.05				—	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	—	0, 5	5	4.95				4.95	5	—	
	—	0, 10	10	9.95				9.95	10	—	
	—	0, 15	15	14.95				14.95	15	—	
Input Low Voltage, V_{IL} Max.	0.5,4.5	—	5	1.5				—	—	1.5	
	1, 9	—	10	3				—	—	3	
	1.5,13.5	—	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	—	5	3.5				3.5	—	—	
	1, 9	—	10	7				7	—	—	
	1.5,13.5	—	15	11				11	—	—	
Input Current, I_{IN} Max.	—	0, 18	18	±0.1	±0.1	±1	±1	—	$\pm 10^{-5}$	±0.1	μA

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operating is always within the following ranges:

CHARACTERISTIC		V_{DD} (V)	LIMITS Min.	LIMITS Max.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		—	3	18	V
Input Pulse Width	$t_{w\phi}$	5	340	—	ns
		10	150	—	
		15	120	—	
Reset Pulse Width	$t_{w(R)}$	5	180	—	
		10	80	—	
		15	50	—	
Input Pulse Frequency	$f\phi$	5	—	2	MHz
		10	—	5	
		15	—	6.5	
Input Pulse Rise or Fall Time	$t_r\phi, t_f\phi$	5	—	15	μs
		10	—	15	
		15	—	15	
R_T Operating Range		5	1K	10M	Ω
		10	1K	10M	
		15	1K	10M	
C_T Operating Range		5	15p	10M	F
		10	15p	10M	
		15	15p	10M	

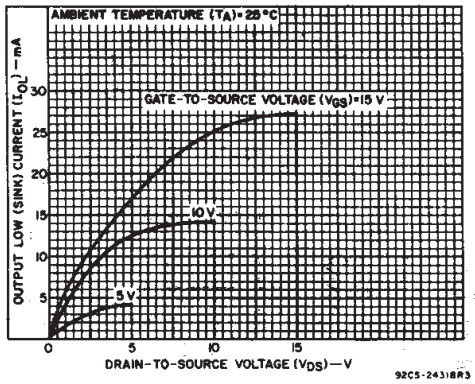


Fig. 2 - Typical output low (sink) current characteristics.

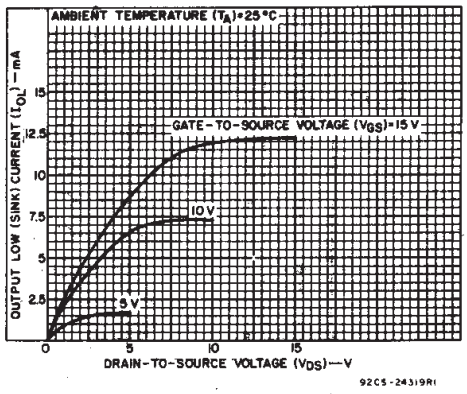


Fig. 3 - Minimum output low (sink) current characteristics.

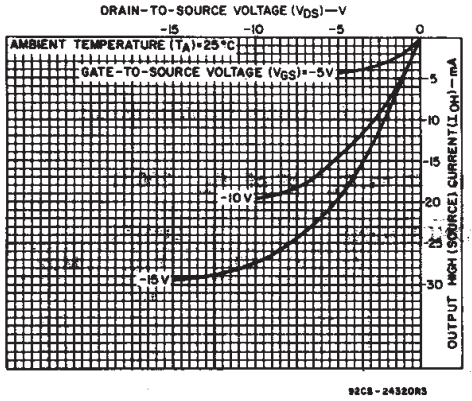


Fig. 4 - Typical output high (source) current characteristics.

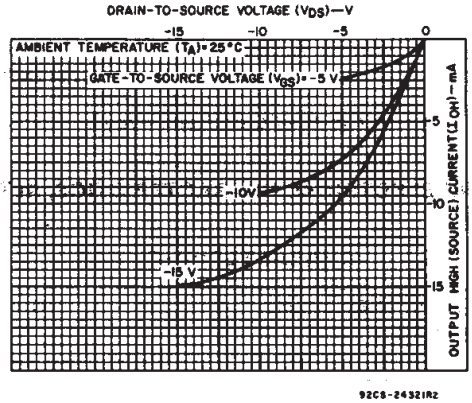


Fig. 5 - Minimum output high (source) current characteristics.

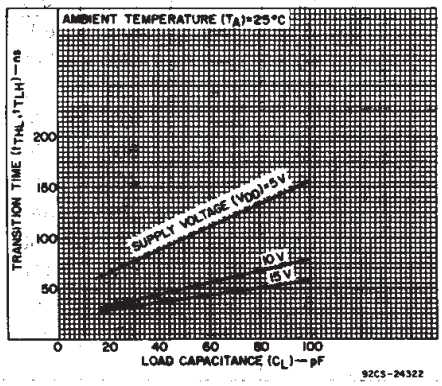


Fig. 6 - Typical transition time as a function of load capacitance.

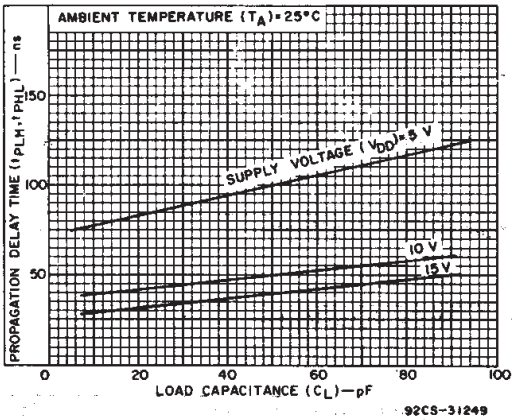


Fig. 7 - Typical propagation delay time (Q_n to $Q_n + 1$) as a function of load capacitance.

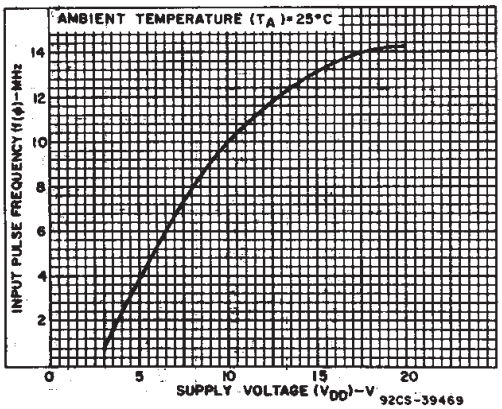


Fig. 8 - Typical maximum input pulse frequency vs. supply voltage.

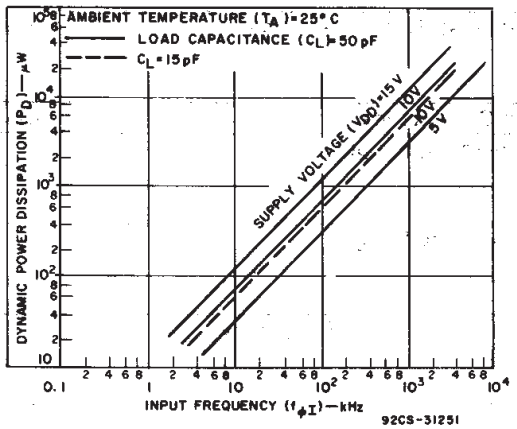


Fig. 9 - Typical dynamic power dissipation as a function of input frequency.

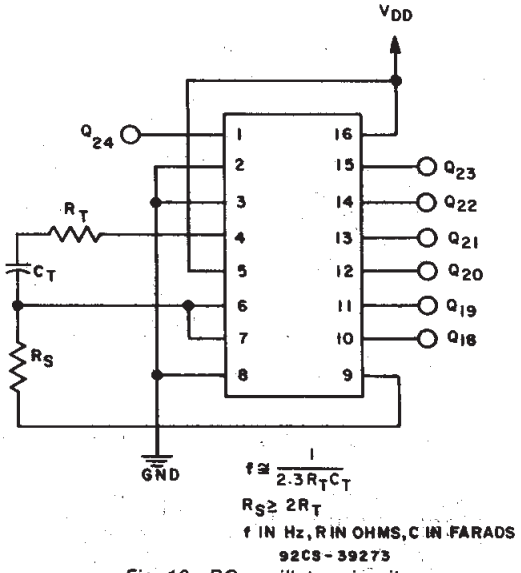


Fig. 10 - RC oscillator circuit.

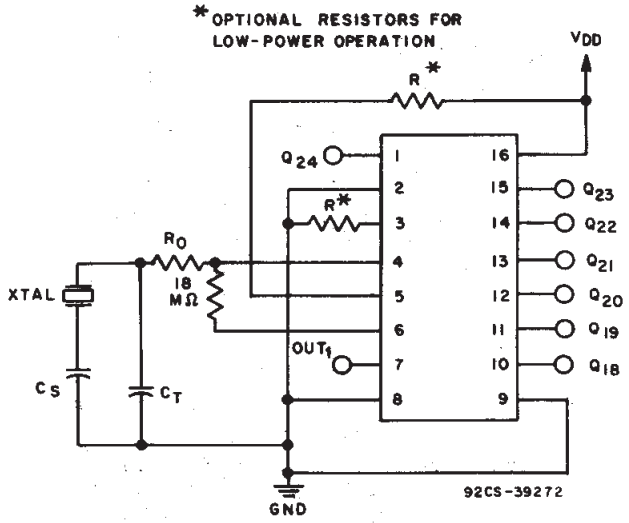


Fig. 11 - Crystal oscillator circuit.

DYNAMIC ELECTRICAL CHARACTERISTICS, At T_A = 25° C; Input t_r,t_f = 20 ns, C_L = 50 pF, R_L = 200 Ω

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			V_{DD}(V)	Min.	Typ.	Max.	
Propagation Delay Time: Input to Q18	t_{PLH}, t_{PHL}		5	—	4.5	9	μs
			10	—	1.7	3.5	
			15	—	1.3	2.7	
Input to Q24			5	—	6	12	
			10	—	2.2	4.5	
			15	—	1.7	3.5	
Reset to Qn			5	—	400	800	ns
			10	—	170	340	
			15	—	120	240	
Transition Time*	t_{THL}, t_{TLH}		5	—	100	200	
			10	—	50	100	
			15	—	40	80	
Minimum Input Pulse Width	$t_{w\phi}$		5	—	170	340	
			10	—	75	150	
			15	—	60	120	
Minimum Reset Pulse Width	$t_{w(R)}$		5	—	90	180	
			10	—	40	80	
			15	—	25	50	
Maximum Input Pulse Frequency	$f\phi$		5	2	4	—	MHz
			10	5	10	—	
			15	6.5	13	—	
Input Pulse Rise or Fall Time	$t_r\phi$, $t_f\phi$		5	—	—	15	μs
			10	—	—	15	
			15	—	—	15	
Input Capacitance	C_{IN}	Any Input		—	5	7.5	pF
R_T Operating Range			5	1K	—	10M	Ω
			10	1K	—	10M	
			15	1K	—	10M	
C_T Operating Range			5	15p	—	10μ	F
			10	15p	—	10μ	
			15	15p	—	10μ	
Maximum Oscillator Frequency		R_T=1 KΩ	5	0.5	0.7	0.9	MHz
		C_T=15 pF	10	1.2	1.5	1.8	
		R_S=30 KΩ	15	1.7	2.1	2.5	

*Not applicable for pin 4 (OUT2).

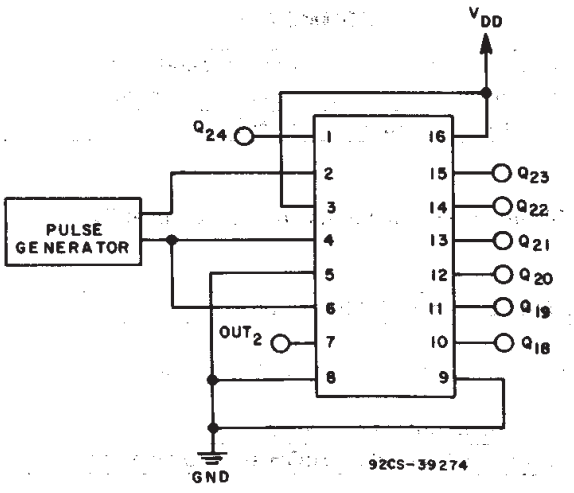


Fig. 12 - Functional test circuit.

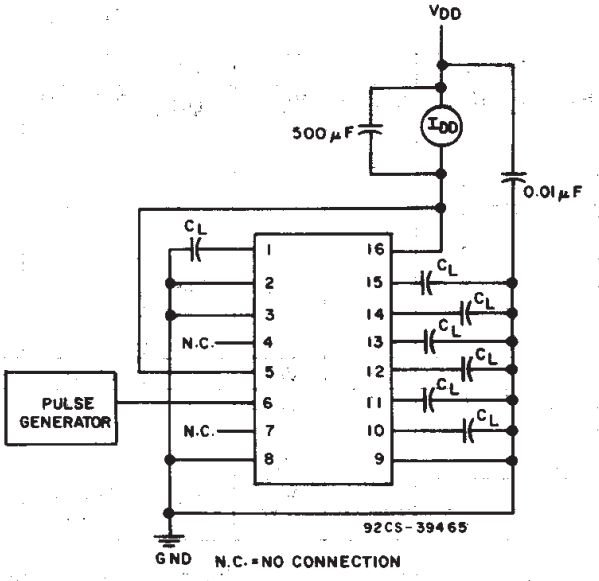


Fig. 13 - Dynamic power dissipation test circuit.

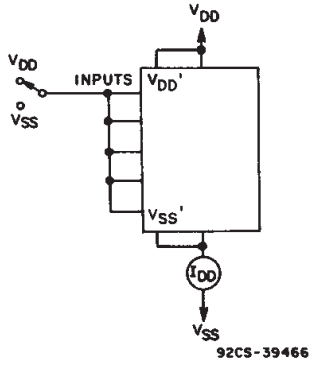


Fig. 14 - Quiescent device current.

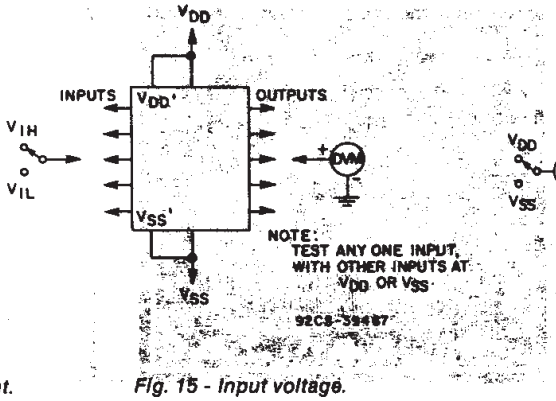


Fig. 15 - Input voltage.

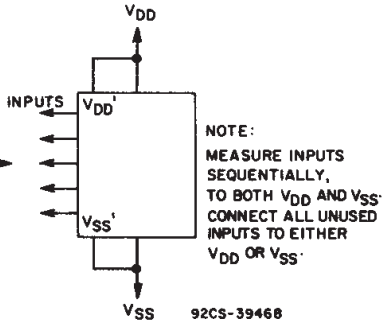
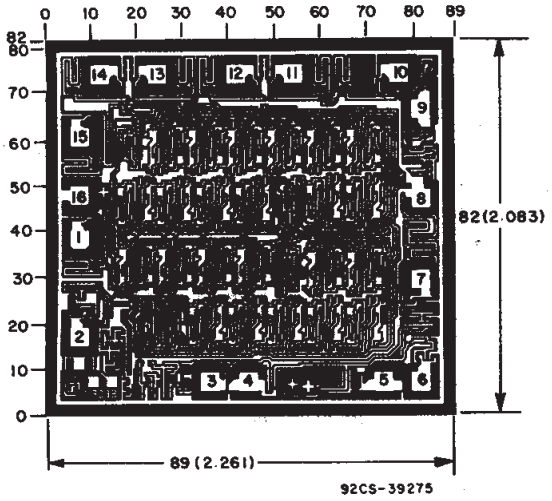


Fig. 16 - Input current.

FUNCTIONAL TEST SEQUENCE

INPUTS		OUTPUTS				COMMENTS
RESET	IN 2	OUT 2	V_{SS}'	V_{DD}'	Q18-Q24	
1	0	0	V_{DD}	V_{SS}	LOW	Counter is in three 8-stage sections in parallel mode. Counter is reset. IN 2 and OUT 2 are tied together.
0	1	1	V_{DD}	V_{SS}		First LOW-to-HIGH transition at IN 2.
0	0 1 — — —	0 1 — — —	V_{DD}	V_{SS}		255 LOW-to-HIGH transitions are clocked in at IN 2.
0	1	1	V_{DD}	V_{SS}	HIGH	The 255th LOW-to-HIGH transition.
0	0	0	V_{DD}	V_{SS}	HIGH	Counter is converted back to 24-stage serial-mode operation.
0	0	0	V_{SS}	V_{SS}	HIGH	
0	1	0	V_{SS}	V_{DD}	HIGH	
0	1		V_{SS}	V_{DD}	HIGH	OUT 2 reverts to output operation.
0	0		V_{SS}	V_{DD}	LOW	Counter ripples from an all-HIGH state to an all-LOW state.

A test function, which divides, has been included to reduce the time required to test all 24 stages of the counter. Three sections are loaded in parallel to 255 counts, forcing all the outputs to be in the HIGH state. The counter is changed back to serial-mode operation and one additional LOW-to-HIGH transition is entered at IN 2, which causes the outputs to ripple from an all-HIGH state to an all-LOW state.



Dimensions and pad layout for CD4521BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
CD4521BE	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD4521BE	Samples
CD4521BEE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD4521BE	Samples
CD4521BM	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4521BM	Samples
CD4521BM96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4521BM	Samples
CD4521BM96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4521BM	Samples
CD4521BM96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4521BM	Samples
CD4521BME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4521BM	Samples
CD4521BMG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4521BM	Samples
CD4521BMT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4521BM	Samples
CD4521BMTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4521BM	Samples
CD4521BMTG4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4521BM	Samples
CD4521BNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4521B	Samples
CD4521BNSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4521B	Samples
CD4521BNSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4521B	Samples
CD4521BPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM521B	Samples
CD4521BPWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM521B	Samples
CD4521BPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM521B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

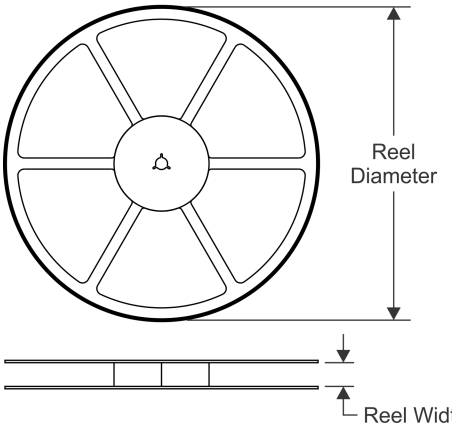
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

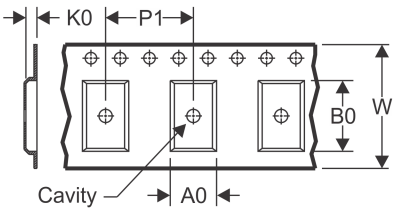
(4) Only one of markings shown within the brackets will appear on the physical device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

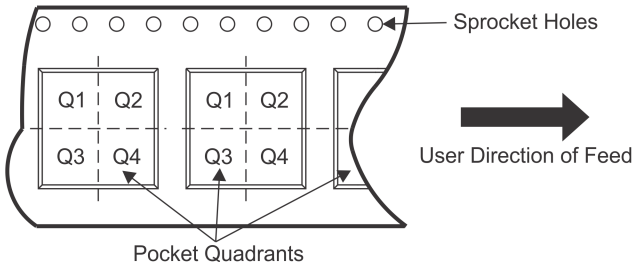


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

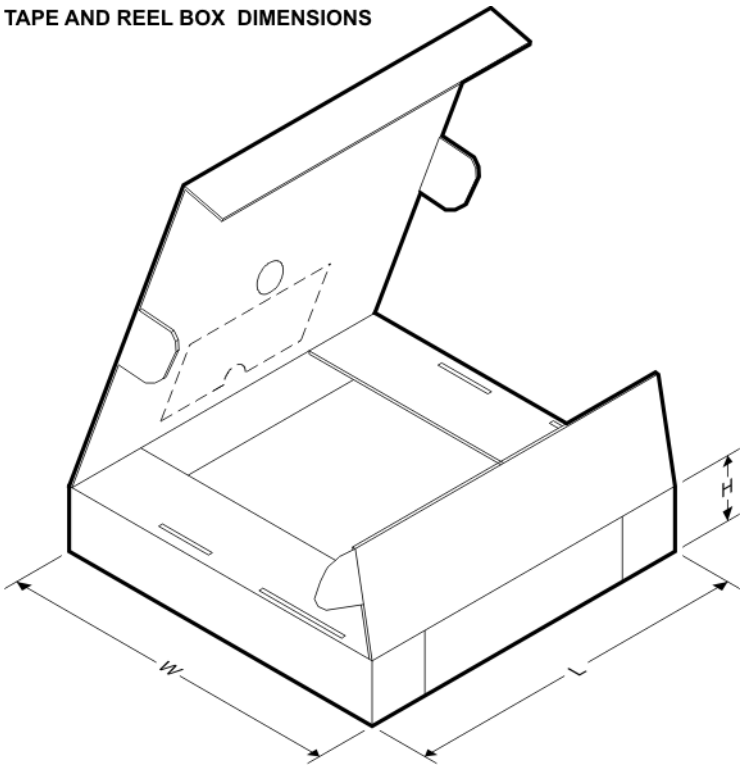
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4521BM96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4521BNSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



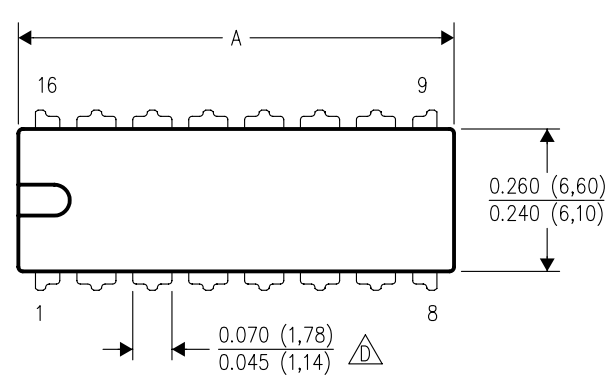
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4521BM96	SOIC	D	16	2500	333.2	345.9	28.6
CD4521BNSR	SO	NS	16	2000	367.0	367.0	38.0

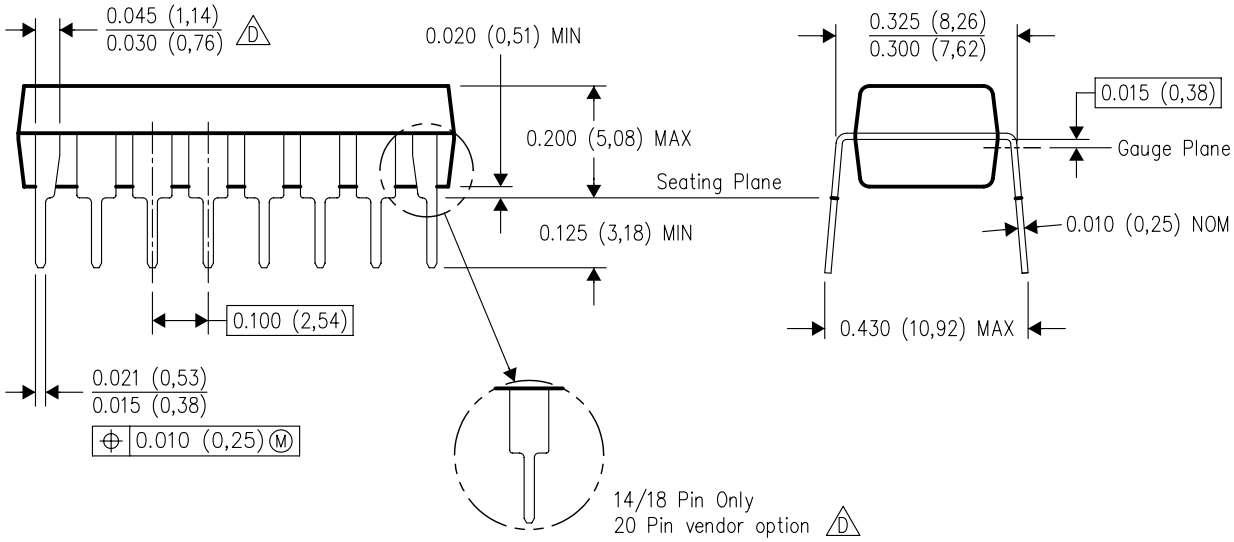
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



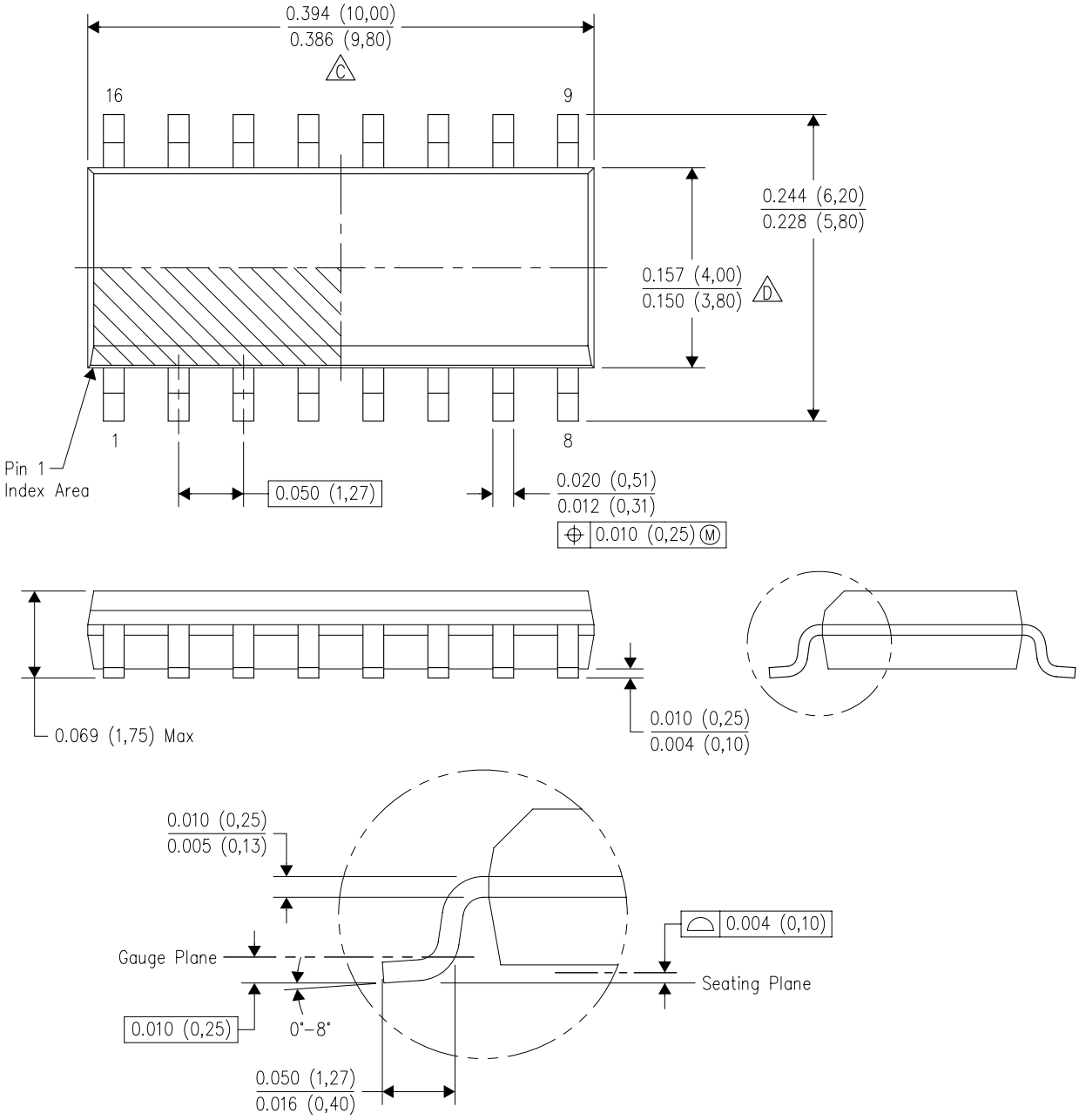
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

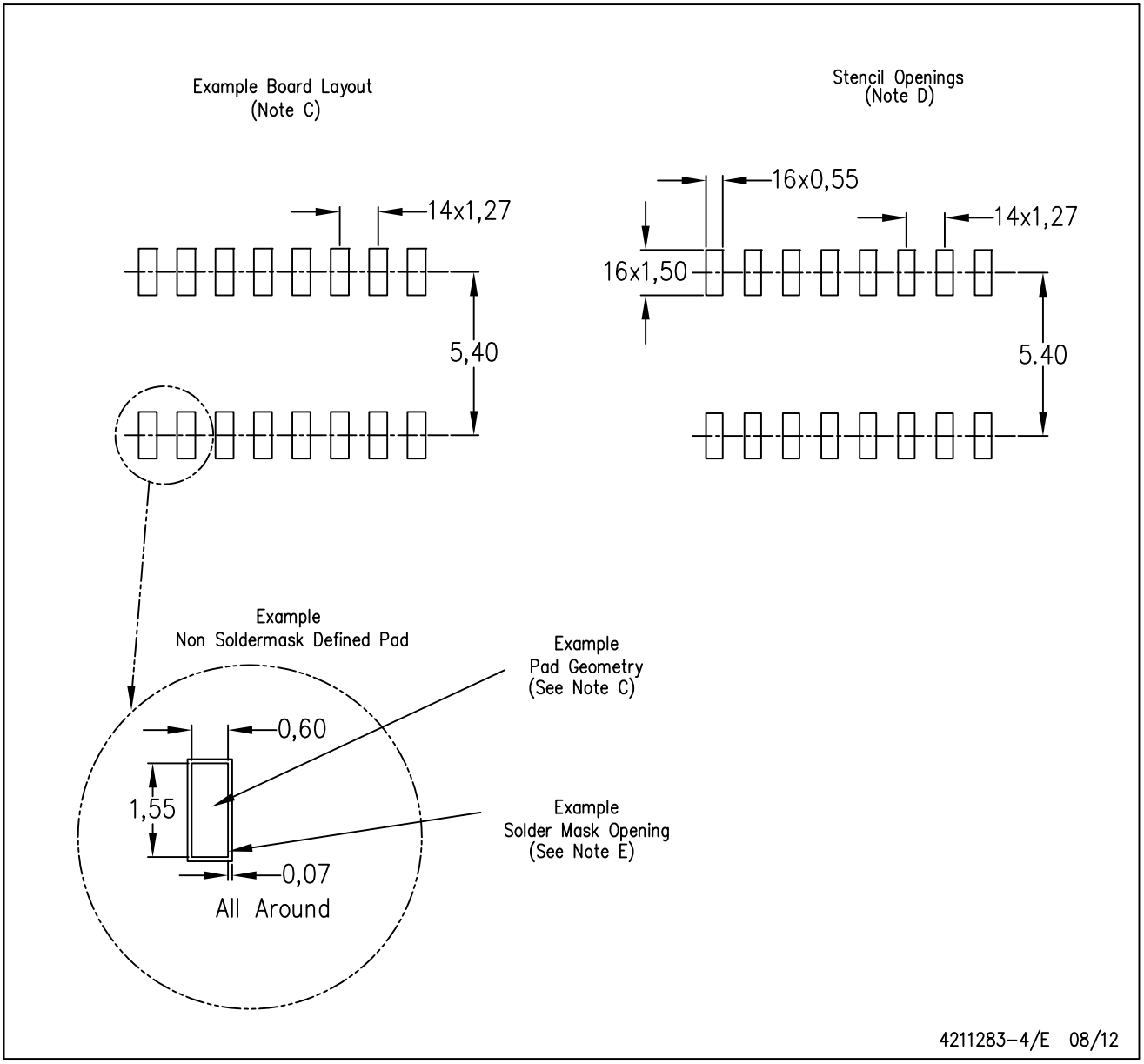
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



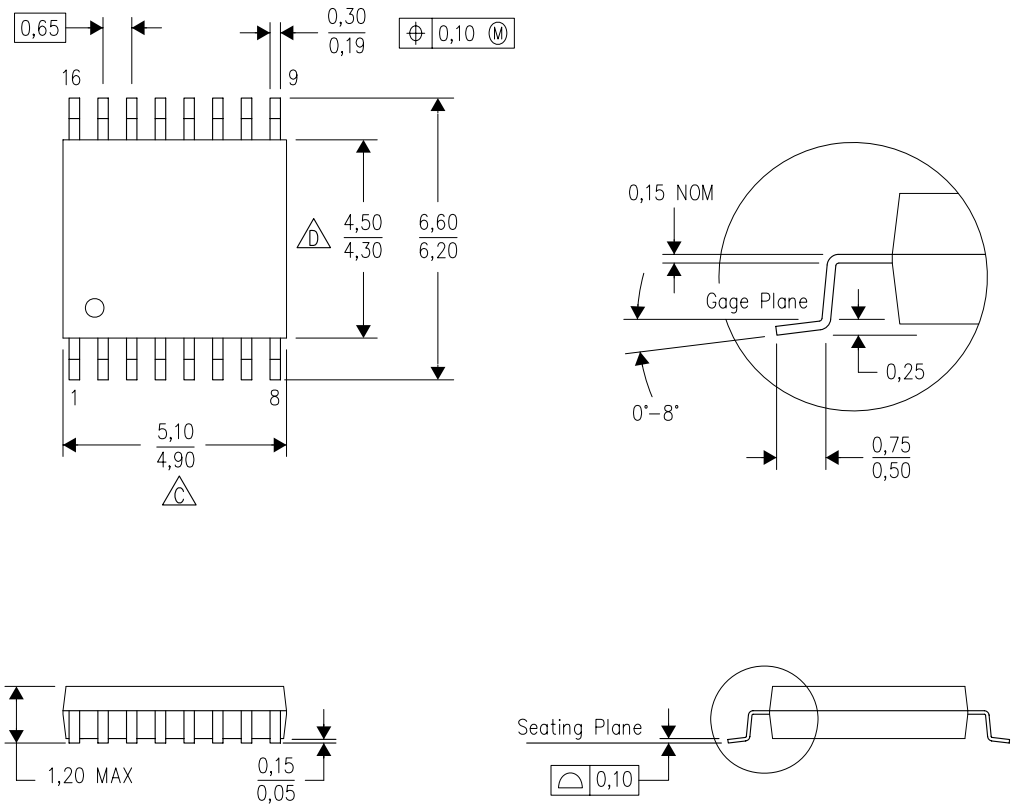
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

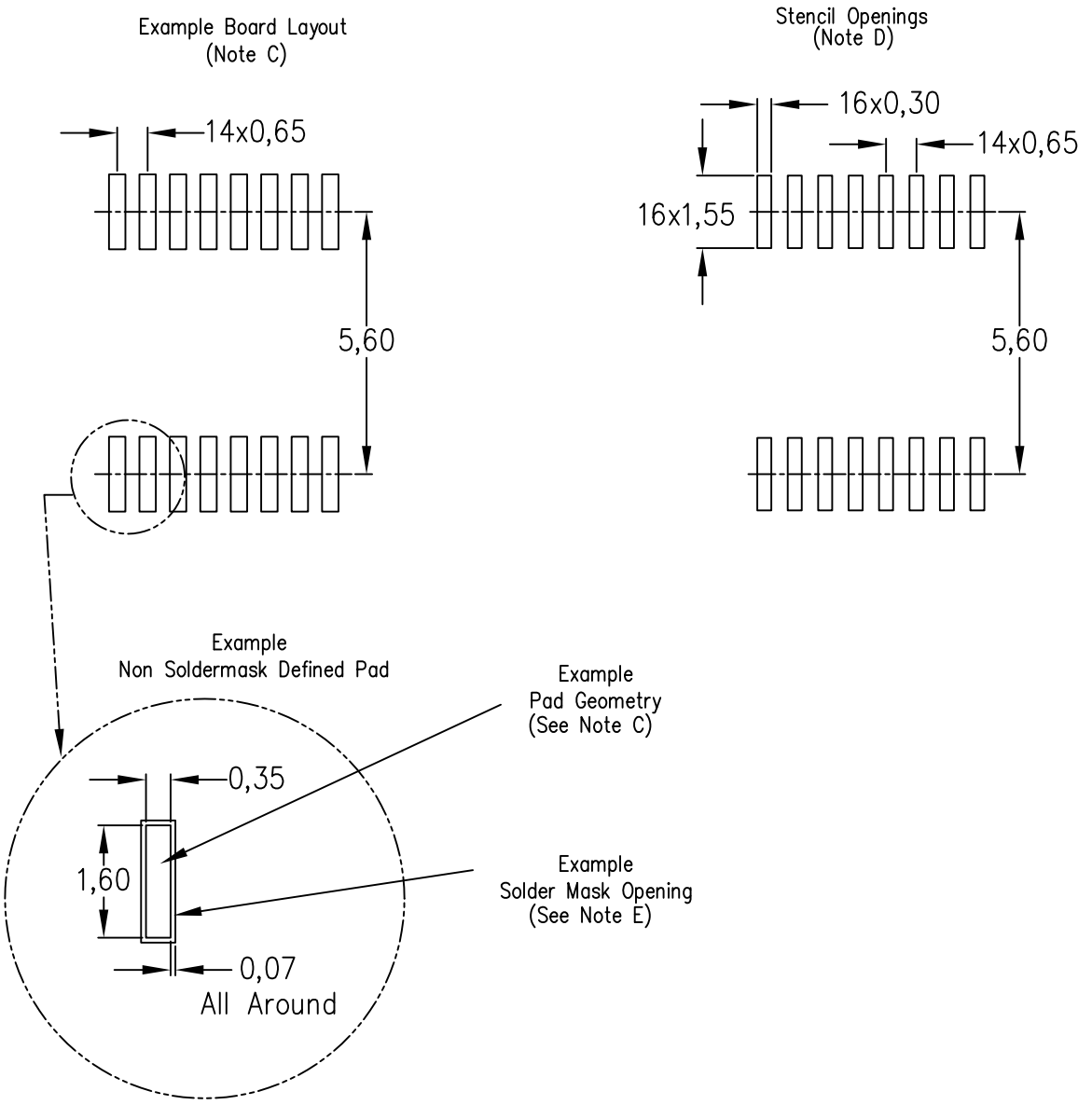
PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



4040064–4/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE

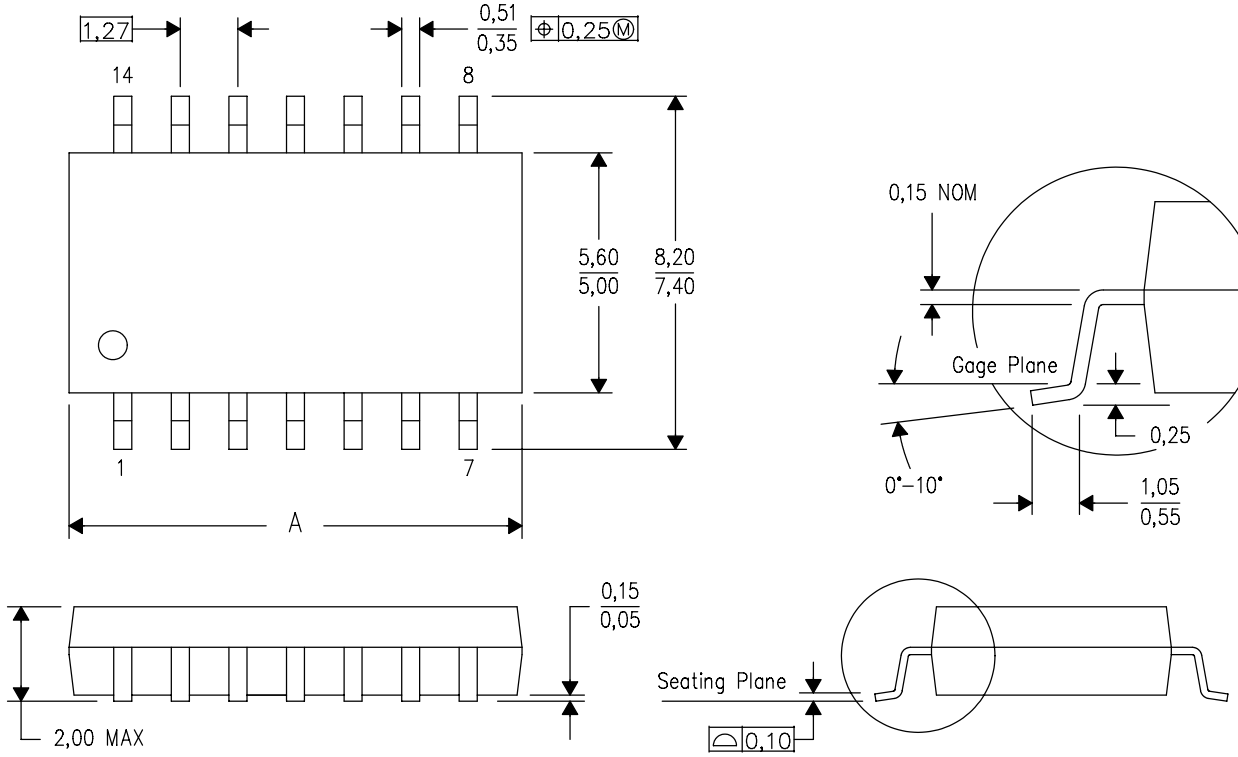


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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