

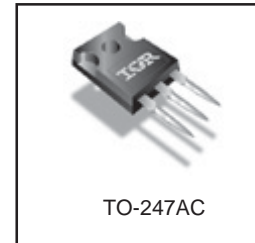
**Applications**

- Zero Voltage Switching SMPS
- Telecom and Server Power Supplies
- Uninterruptible Power Supplies
- Motor Control applications

V <sub>DSS</sub>	R <sub>DS(on) typ.</sub>	T <sub>rr typ.</sub>	I <sub>D</sub>
600V	210mΩ	170ns	26A

**Features and Benefits**

- SuperFast body diode eliminates the need for external diodes in ZVS applications.
- Lower Gate charge results in simpler drive requirements.
- Enhanced dv/dt capabilities offer improved ruggedness.
- Higher Gate voltage threshold offers improved noise immunity.



**Absolute Maximum Ratings**

	Parameter	Max.	Units
I <sub>D</sub> @ T <sub>C</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V	26	A
I <sub>D</sub> @ T <sub>C</sub> = 100°C	Continuous Drain Current, V <sub>GS</sub> @ 10V	17	
I <sub>DM</sub>	Pulsed Drain Current ①	100	
P <sub>D</sub> @ T <sub>C</sub> = 25°C	Power Dissipation	470	W
	Linear Derating Factor	3.8	W/°C
V <sub>GS</sub>	Gate-to-Source Voltage	±30	V
dv/dt	Peak Diode Recovery dv/dt ②	30	V/ns
T <sub>J</sub>	Operating Junction and	-55 to + 150	°C
T <sub>STG</sub>	Storage Temperature Range		
	Soldering Temperature, for 10 seconds		
	Mounting torque, 6-32 or M3 screw	1.1(10)	N•m (lbf•in)

**Diode Characteristics**

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	26	A	MOSFET symbol showing the integral reverse p-n junction diode.
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	100		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.5	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 26A, V <sub>GS</sub> = 0V ④
t <sub>rr</sub>	Reverse Recovery Time	—	170	250	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = 26A
		—	210	320		T <sub>J</sub> = 125°C, di/dt = 100A/μs ④
Q <sub>rr</sub>	Reverse Recovery Charge	—	670	1000	nC	T <sub>J</sub> = 25°C, I <sub>S</sub> = 26A, V <sub>GS</sub> = 0V ④
		—	1050	1570		T <sub>J</sub> = 125°C, di/dt = 100A/μs ④
I <sub>RSM</sub>	Reverse Recovery Current	—	7.3	11	A	T <sub>J</sub> = 25°C
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

## Static @ T<sub>J</sub> = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	600	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔV <sub>(BR)DSS/ΔT<sub>J</sub></sub>	Breakdown Voltage Temp. Coefficient	—	0.33	—	V/°C	Reference to 25°C, I <sub>D</sub> = 1mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	210	250	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 16A ④
V <sub>GS(th)</sub>	Gate Threshold Voltage	3.0	—	5.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	50	μA	V <sub>DS</sub> = 600V, V <sub>GS</sub> = 0V
		—	—	2.0	mA	V <sub>DS</sub> = 480V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> = 30V
	Gate-to-Source Reverse Leakage	—	—	-100	nA	V <sub>GS</sub> = -30V
R <sub>G</sub>	Internal Gate Resistance	—	0.8	—	Ω	f = 1MHz, open drain

## Dynamic @ T<sub>J</sub> = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
g <sub>fs</sub>	Forward Transconductance	13	—	—	S	V <sub>DS</sub> = 50V, I <sub>D</sub> = 16A
Q <sub>g</sub>	Total Gate Charge	—	—	180	nC	I <sub>D</sub> = 26A V <sub>DS</sub> = 480V V <sub>GS</sub> = 10V, See Fig. 7 & 15 ④
Q <sub>gs</sub>	Gate-to-Source Charge	—	—	61		
Q <sub>gd</sub>	Gate-to-Drain ("Miller") Charge	—	—	85		
t <sub>d(on)</sub>	Turn-On Delay Time	—	31	—	ns	V <sub>DD</sub> = 300V I <sub>D</sub> = 26A R <sub>G</sub> = 4.3Ω V <sub>GS</sub> = 10V, See Fig. 11a & 11b ④
t <sub>r</sub>	Rise Time	—	110	—		
t <sub>d(off)</sub>	Turn-Off Delay Time	—	47	—		
t <sub>f</sub>	Fall Time	—	42	—		
C <sub>iss</sub>	Input Capacitance	—	5020	—	pF	V <sub>GS</sub> = 0V V <sub>DS</sub> = 25V f = 1.0MHz, See Fig. 5 V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 480V ⑤
C <sub>oss</sub>	Output Capacitance	—	450	—		
C <sub>rss</sub>	Reverse Transfer Capacitance	—	34	—		
C <sub>oss eff.</sub>	Effective Output Capacitance	—	230	—		
C <sub>oss eff. (ER)</sub>	Effective Output Capacitance (Energy Related)	—	170	—		

## Avalanche Characteristics

Symbol	Parameter	Typ.	Max.	Units
E <sub>AS</sub>	Single Pulse Avalanche Energy ②	—	570	mJ
I <sub>AR</sub>	Avalanche Current ①	—	26	A
E <sub>AR</sub>	Repetitive Avalanche Energy ①	—	47	mJ

## Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
R <sub>θJC</sub>	Junction-to-Case ⑥	—	0.27	°C/W
R <sub>θCS</sub>	Case-to-Sink, Flat, Greased Surface	0.24	—	
R <sub>θJA</sub>	Junction-to-Ambient ⑥	—	40	

### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See Fig. 12)
- ② Starting T<sub>J</sub> = 25°C, L = 1.7mH, R<sub>G</sub> = 25Ω, I<sub>AS</sub> = 26A, (See Figure 14a)
- ③ I<sub>SD</sub> ≤ 26A, di/dt ≤ 719A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>, T<sub>J</sub> ≤ 150°C.

④ Pulse width ≤ 300μs; duty cycle ≤ 2%.

⑤ C<sub>oss eff.</sub> is a fixed capacitance that gives the same charging time as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>DSS</sub>.  
C<sub>oss eff.(ER)</sub> is a fixed capacitance that stores the same energy as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>DSS</sub>.

⑥ R<sub>θ</sub> is measured at T<sub>J</sub> approximately 90°C

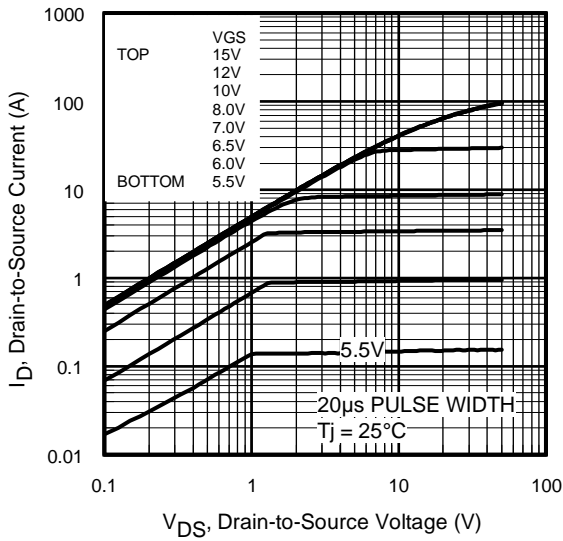


Fig 1. Typical Output Characteristics

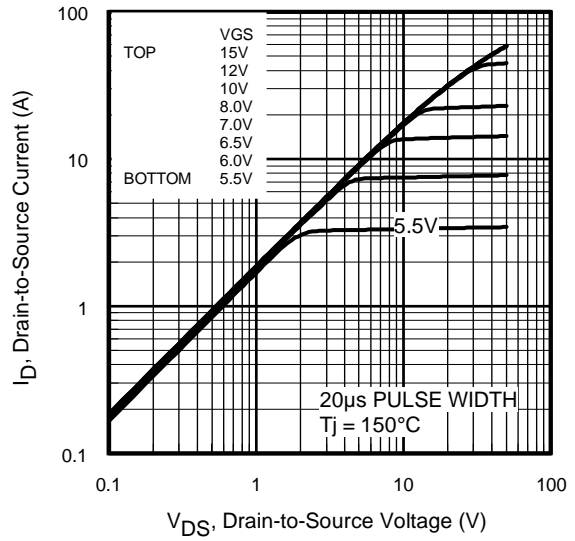


Fig 2. Typical Output Characteristics

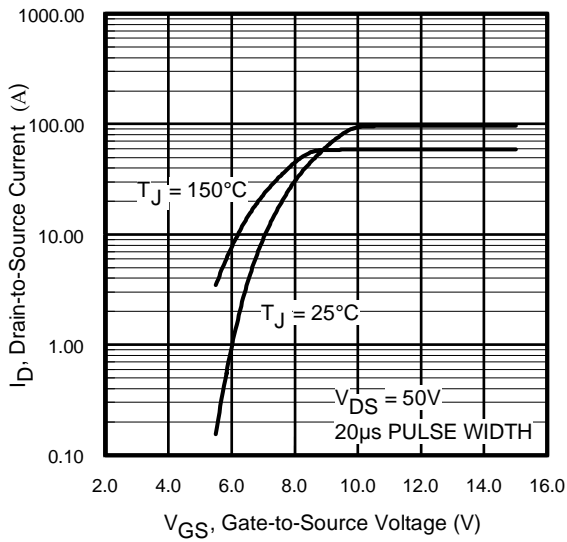


Fig 3. Typical Transfer Characteristics

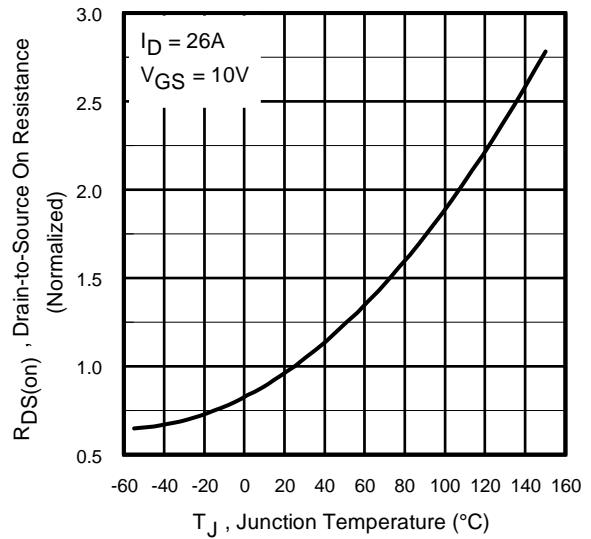
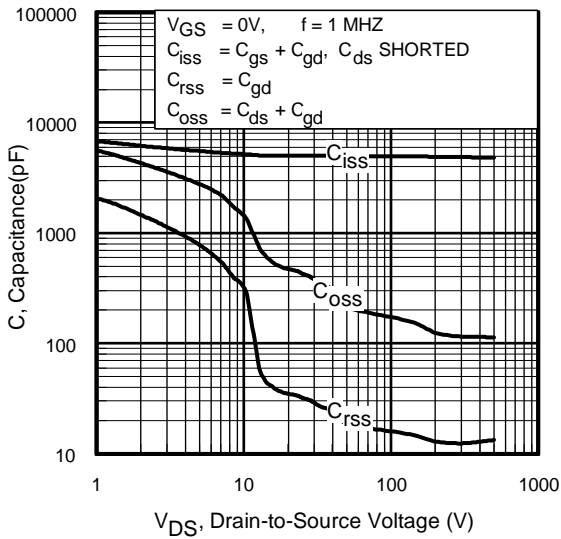
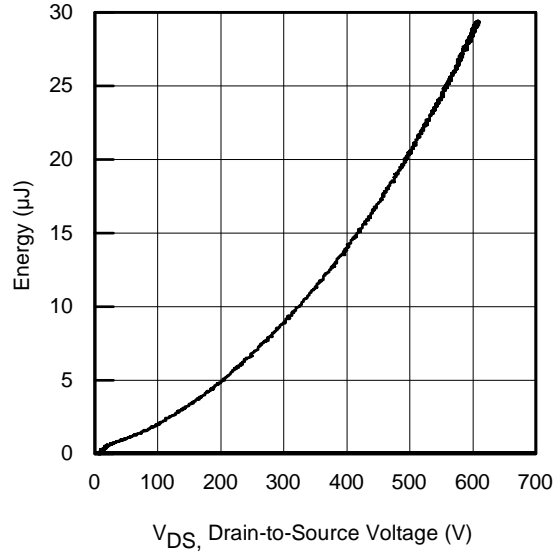


Fig 4. Normalized On-Resistance Vs. Temperature

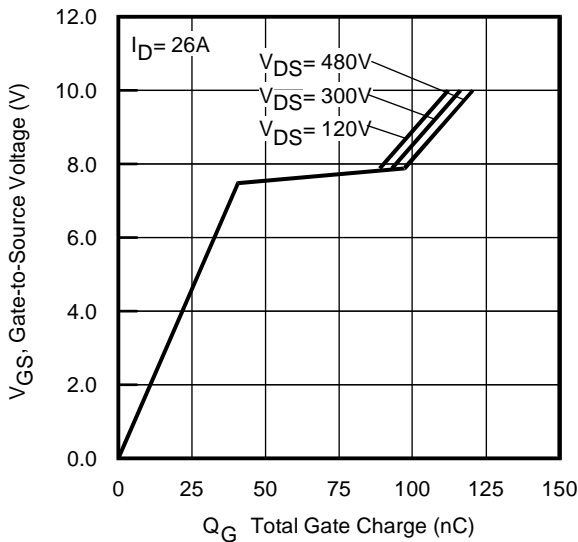
# IRFP26N60L



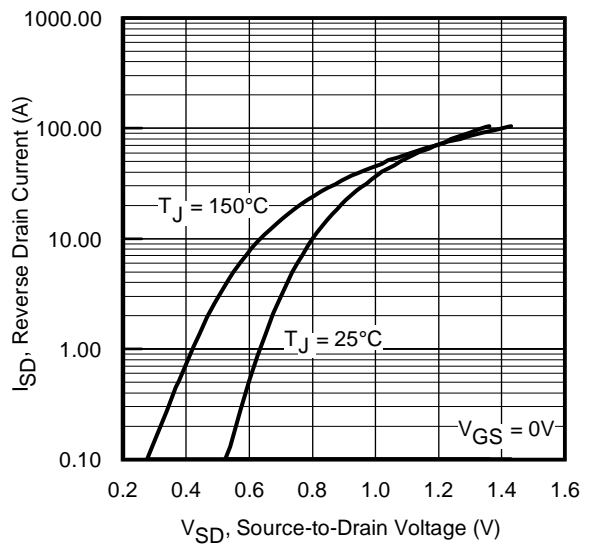
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



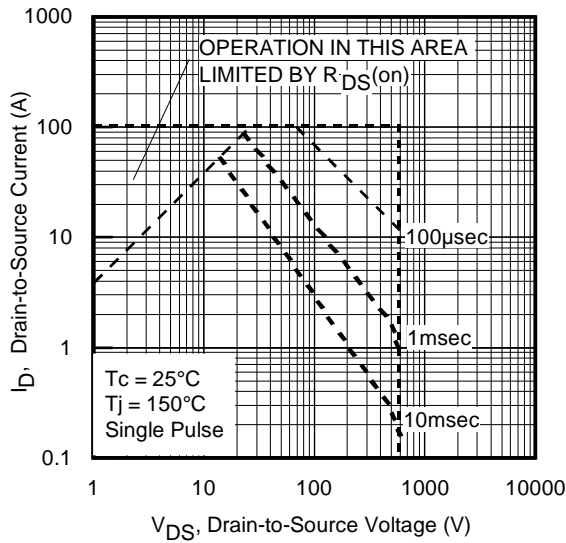
**Fig 6.** Typ. Output Capacitance Stored Energy vs.  $V_{DS}$



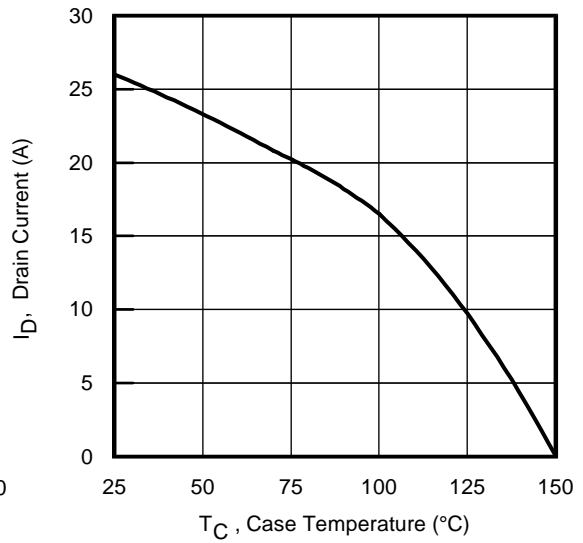
**Fig 7.** Typical Gate Charge Vs. Gate-to-Source Voltage



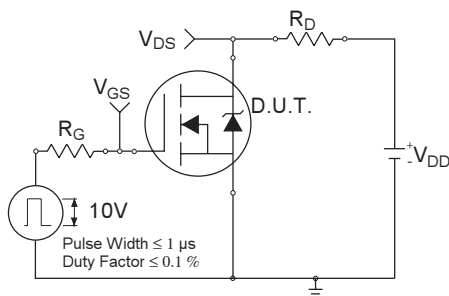
**Fig 8.** Typical Source-Drain Diode Forward Voltage



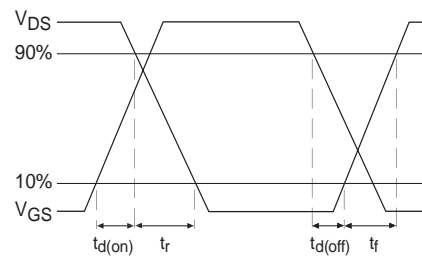
**Fig 9.** Maximum Safe Operating Area



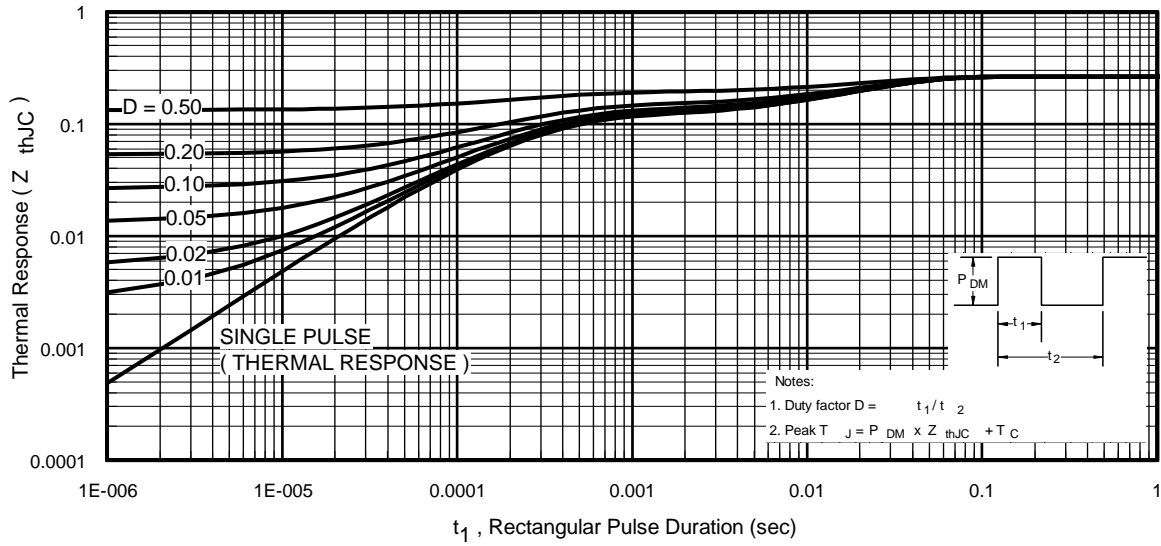
**Fig 10.** Maximum Drain Current vs. Case Temperature



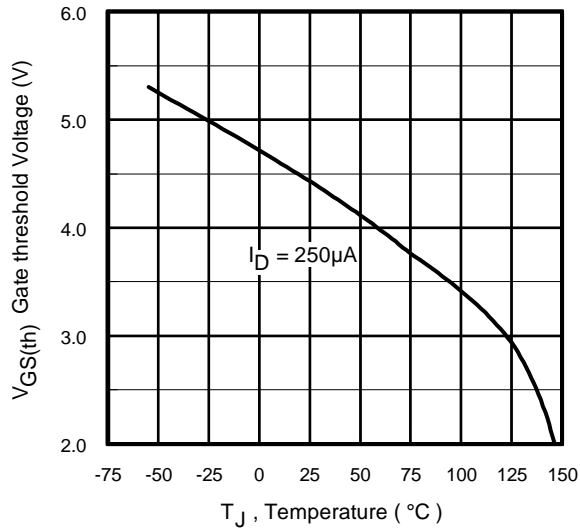
**Fig 11a.** Switching Time Test Circuit



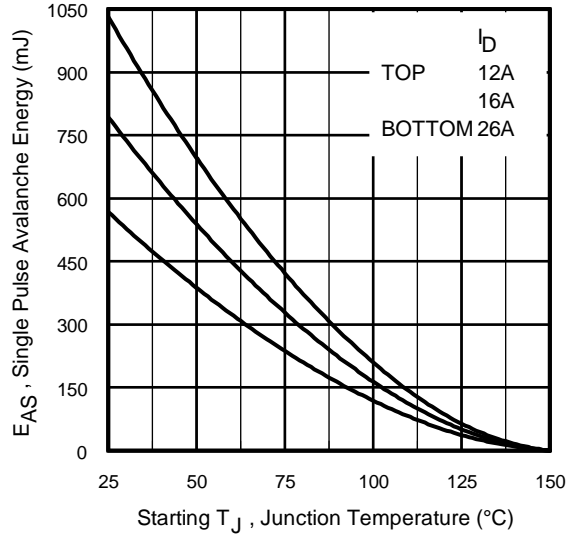
**Fig 11b.** Switching Time Waveforms



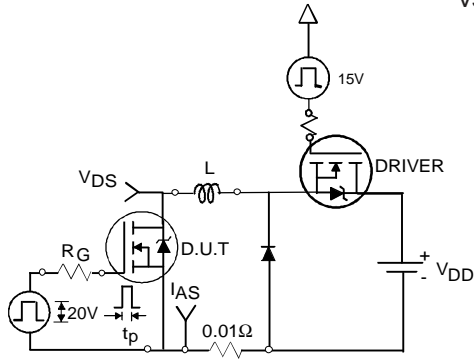
**Fig 12.** Maximum Effective Transient Thermal Impedance, Junction-to-Case



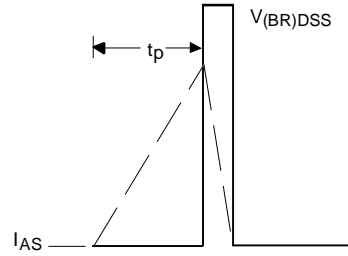
**Fig 13.** Threshold Voltage vs. Temperature



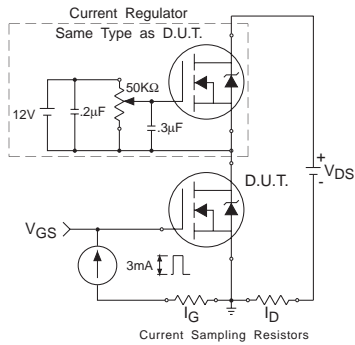
**Fig 14a.** Maximum Avalanche Energy vs. Drain Current



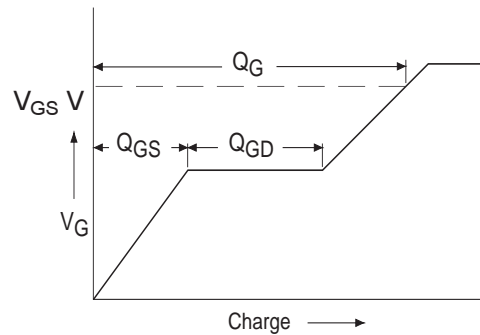
**Fig 14b.** Unclamped Inductive Test Circuit



**Fig 14c.** Unclamped Inductive Waveforms

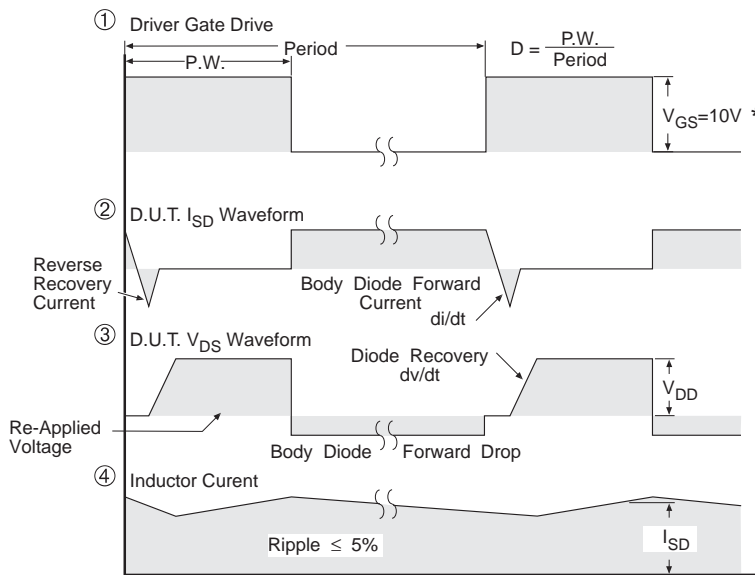
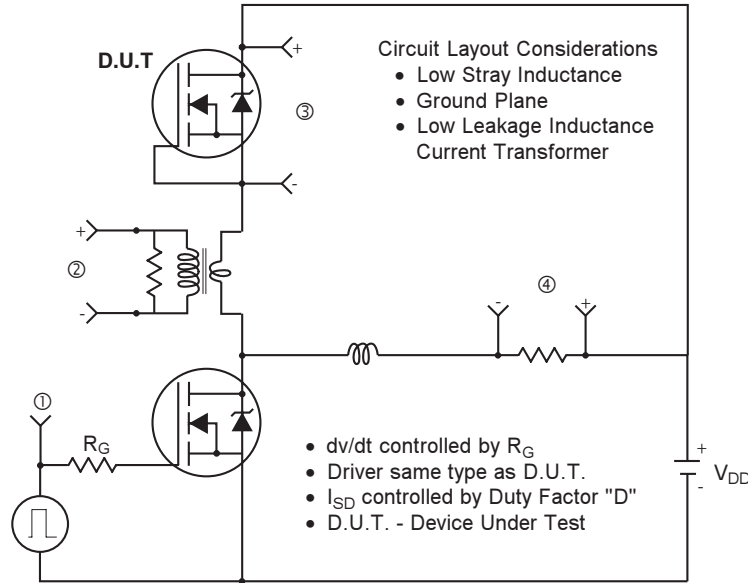


**Fig 15a.** Gate Charge Test Circuit



**Fig 15b.** Basic Gate Charge Waveform

## Peak Diode Recovery dv/dt Test Circuit

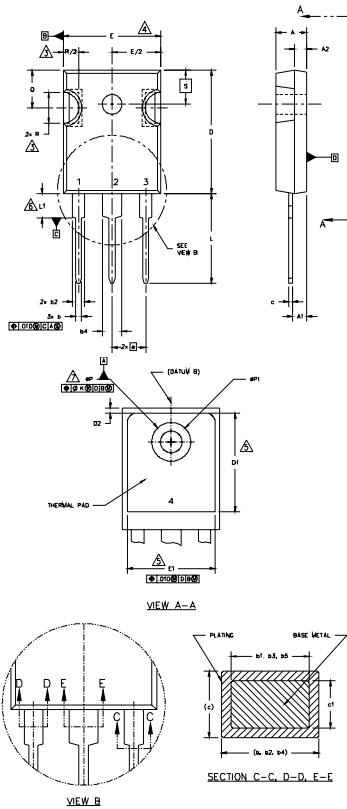


\*  $V_{GS} = 5V$  for Logic Level Devices

**Fig 16.** For N-Channel HEXFET® Power MOSFETs



TO-247AC Package Outline Dimensions are shown in millimeters (inches)



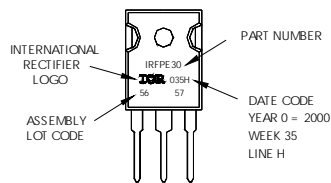
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M 1994.
2. DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS]
3. CONTOUR OF SLOT OPTIONAL.
4. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS D1 & E1.
6. LEAD FINISH UNCONTROLLED IN L1.
7. #P TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154" [3.91].
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-247 WITH THE EXCEPTION OF DIMENSION c.

SYMBOL	DIMENSIONS				NOTES	LEAD ASSIGNMENTS
	INCHES		MILLIMETERS			
	MIN.	MAX.	MIN.	MAX.		
A	.183	.209	4.65	5.31		
A1	.087	.102	2.21	2.59		
A2	.059	.098	1.50	2.49		
b	.039	.055	0.99	1.40		<b>HEXFET</b>
b1	.039	.053	0.99	1.35		1.- GATE
b2	.065	.094	1.65	2.39		2.- DRAIN
b3	.065	.092	1.65	2.37		3.- SOURCE
b4	.102	.135	2.59	3.43		4.- DRAIN
b5	.102	.133	2.59	3.38		
c	.015	.034	0.38	0.86		<b>IGBTs, CoPACK</b>
c1	.015	.030	0.38	0.76	4	1.- GATE
D	.776	.815	19.71	20.70	5	2.- COLLECTOR
D1	.515	-	13.08	-		3.- EMITTER
D2	.020	.030	0.51	0.76	4	4.- COLLECTOR
E	.602	.625	15.29	15.87		
E1	.540	-	15.72	-		
e	.215 BSC		5.46 BSC			
ek	.010		2.54			
L	.559	.634	14.20	16.10		<b>DIODES</b>
L1	.146	.169	3.71	4.29		1.- ANODE/OPEN
N	3		7.62 BSC			2.- CATHODE
#P	.140	.144	3.56	3.66		3.- ANODE
øP1	-	.275	-	6.98		
Q	.209	.224	5.31	5.69		
R	.178	.216	4.52	5.49		
S	.217 BSC		5.51 BSC			

## TO-247AC Part Marking Information

EXAMPLE: THIS IS AN IRFPE30 WITH ASSEMBLY LOT CODE 5657 ASSEMBLED ON WW 35, 2000 IN THE ASSEMBLY LINE "H"  
**Note:** "P" in assembly line position indicates "Lead-Free"



**TO-247AC package is not recommended for Surface Mount Application.**

Data and specifications subject to change without notice. This product has been designed and qualified for the Industrial market. Qualification Standards can be found on IR's Web site.