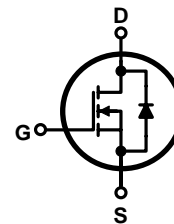
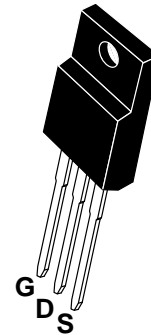
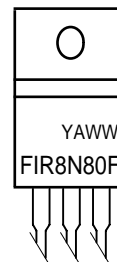


**PIN Connection TO-220F**
**Switching Regulator Application**
**Features**

- High voltage:  $BV_{DSS}=800V$
- Low gate charge:  $Q_g=40nC$  (Typ.)
- Low drain-source On resistance:  $R_{DS(on)}=1.6\Omega$  (Max.)
- 100% avalanche tested
- RoHS compliant device and available in halogen free device


**Marking Diagram**


- Y = Year
- A = Assembly Location
- WW = Work Week
- FIR8N80F = Specific Device Code

**Absolute maximum ratings ( $T_c=25^\circ C$  unless otherwise noted)**

Characteristic	Symbol	Rating	Unit	
Drain-source voltage	$V_{DSS}$	800	V	
Gate-source voltage	$V_{GSS}$	$\pm 30$	V	
Drain current (DC) *	$I_D$	$T_c=25^\circ C$	7	A
		$T_c=100^\circ C$	4.4	A
Drain current (Pulsed) *	$I_{DM}$	28	A	
Avalanche current <sup>(Note 2)</sup>	$I_{AS}$	7	A	
Single pulsed avalanche energy <sup>(Note 2)</sup>	$E_{AS}$	522	mJ	
Repetitive avalanche current <sup>(Note 1)</sup>	$I_{AR}$	7	A	
Repetitive avalanche energy <sup>(Note 1)</sup>	$E_{AR}$	4.5	mJ	
Power dissipation	$P_D$	45	W	
Junction temperature	$T_J$	150	$^\circ C$	
Storage temperature range	$T_{stg}$	-55~150	$^\circ C$	

**Thermal Characteristics**

Characteristic	Symbol	Rating	Unit
Thermal resistance, junction to case	$R_{th(j-c)}$	Max. 2.77	°C/W
Thermal resistance, junction to ambient	$R_{th(j-a)}$	Max. 62.5	

**Electrical Characteristics ( $T_C=25^\circ\text{C}$  unless otherwise noted)**

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Drain-source breakdown voltage	$BV_{DSS}$	$I_D=250\mu\text{A}$ , $V_{GS}=0$	800	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$I_D=250\mu\text{A}$ , $V_{DS}=V_{GS}$	3	-	5	V
Drain-source cut-off current	$I_{DSS}$	$V_{DS}=800\text{V}$ , $V_{GS}=0\text{V}$	-	-	1	$\mu\text{A}$
Gate leakage current	$I_{GSS}$	$V_{DS}=0\text{V}$ , $V_{GS}=\pm 30\text{V}$	-	-	$\pm 100$	nA
Drain-source on-resistance	$R_{DS(on)}$	$V_{GS}=10\text{V}$ , $I_D=3.5\text{A}$	-	1.28	1.6	$\Omega$
Forward transfer conductance (Note 3)	$g_{fs}$	$V_{DS}=10\text{V}$ , $I_D=3.5\text{A}$	-	5.6	-	S
Input capacitance	$C_{iss}$	$V_{DS}=25\text{V}$ , $V_{GS}=0\text{V}$ , $f=1.0\text{MHz}$	-	1650	-	pF
Output capacitance	$C_{oss}$		-	135	-	
Reverse transfer capacitance	$C_{rss}$		-	15	-	
Turn-on delay time (Note 3,4)	$t_{d(on)}$	$V_{DD}=400\text{V}$ , $I_D=7\text{A}$ , $R_G=25\Omega$	-	40	-	ns
Rise time (Note 3,4)	$t_r$		-	110	-	
Turn-off delay time (Note 3,4)	$t_{d(off)}$		-	65	-	
Fall time (Note 3,4)	$t_f$		-	70	-	
Total gate charge (Note 3,4)	$Q_g$	$V_{DS}=640\text{V}$ , $V_{GS}=10\text{V}$ , $I_D=7\text{A}$	-	40	-	nC
Gate-source charge (Note 3,4)	$Q_{gs}$		-	12	-	
Gate-drain charge (Note 3,4)	$Q_{gd}$		-	15	-	

**Source-Drain Diode Ratings and Characteristics ( $T_C=25^\circ\text{C}$  unless otherwise noted)**

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Source current (DC)	$I_S$	Integral reverse diode in the MOSFET	-	-	7	A
Source current (Pulsed)	$I_{SM}$		-	-	28	A
Forward voltage	$V_{SD}$	$V_{GS}=0\text{V}$ , $I_S=7\text{A}$	-	-	1.4	V
Reverse recovery time (Note 3,4)	$t_{rr}$	$I_S=7\text{A}$ , $V_{GS}=0\text{V}$ $di_f/dt=100\text{A}/\mu\text{s}$	-	560	-	ns
Reverse recovery charge (Note 3,4)	$Q_{rr}$		-	4	-	$\mu\text{C}$

Note:

1. Repeated rating: Pulse width limited by safe operating area
2.  $L=20\text{mH}$ ,  $I_{AS}=7\text{A}$ ,  $V_{DD}=50\text{V}$ ,  $R_G=25\Omega$ , Starting  $T_J=25^\circ\text{C}$
3. Pulse test: Pulse width  $\leq 300\mu\text{s}$ , Duty cycle  $\leq 2\%$
4. Essentially independent of operating temperature typical characteristics

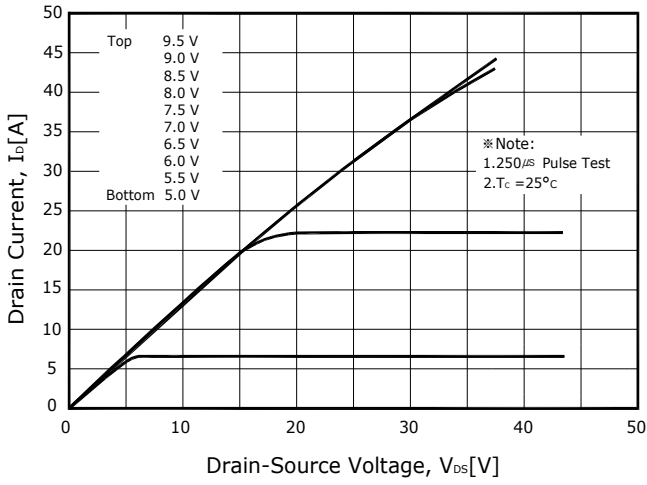
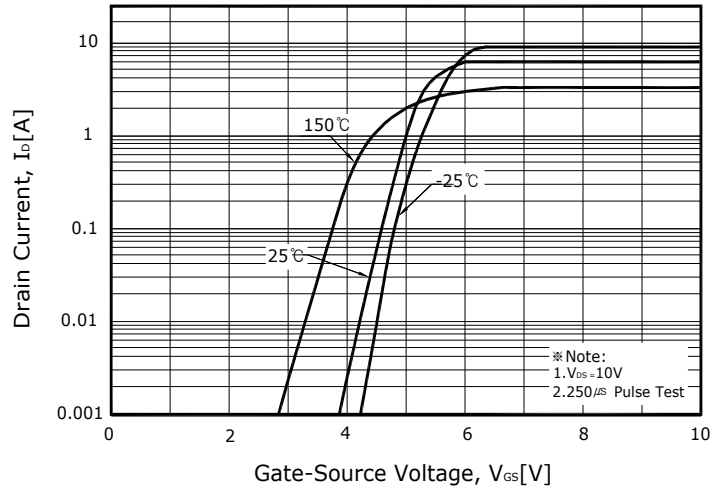
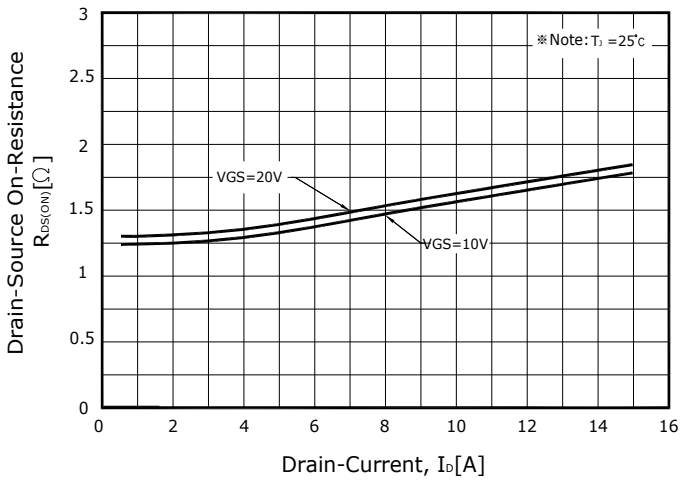
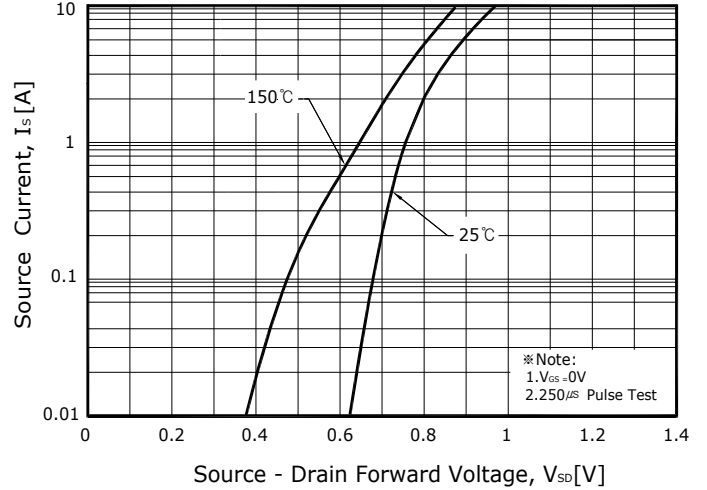
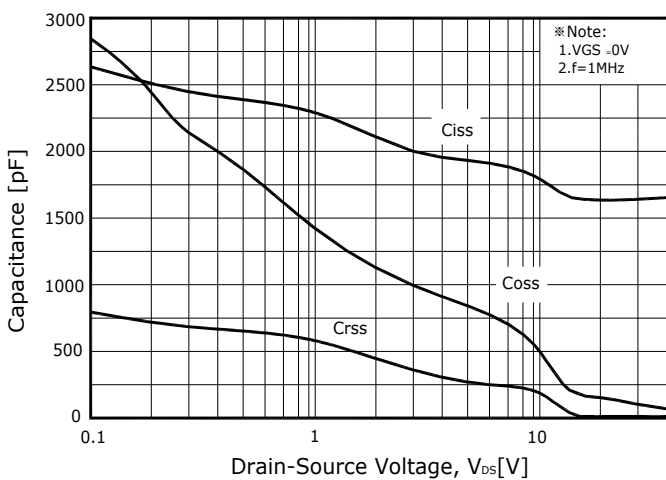
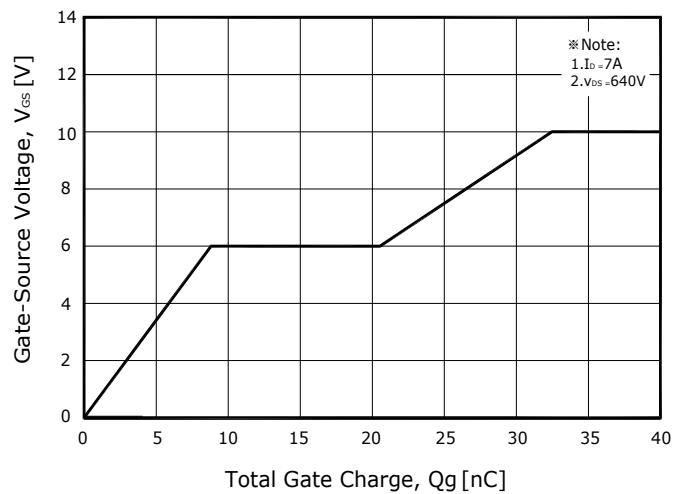
**Electrical Characteristics Curves**
**Fig. 1  $I_D - V_{DS}$** 

**Fig. 2  $I_D - V_{GS}$** 

**Fig. 3  $R_{DS(ON)} - I_D$** 

**Fig. 4  $I_S - V_{SD}$** 

**Fig. 5 Capacitance -  $V_{DS}$** 

**Fig. 6  $V_{GS} - Q_G$** 


Fig. 7  $BV_{DSS} - T_J$

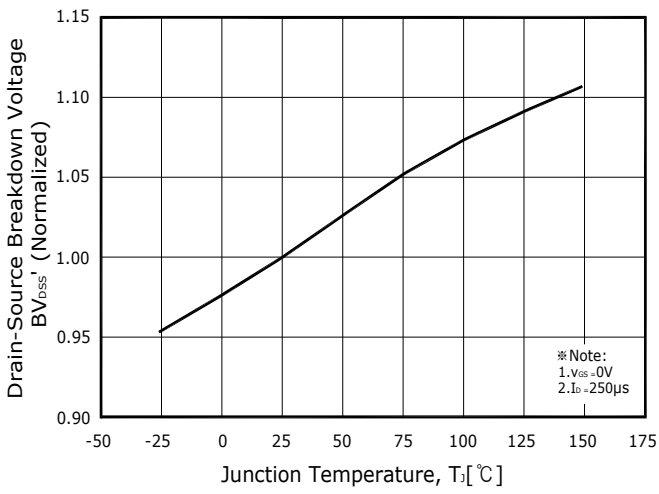


Fig. 8  $R_{DS(on)} - T_J$

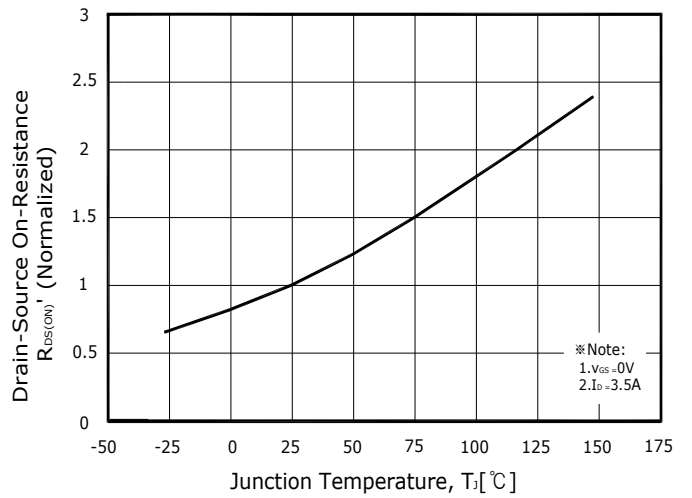


Fig. 9 Safe Operating Area

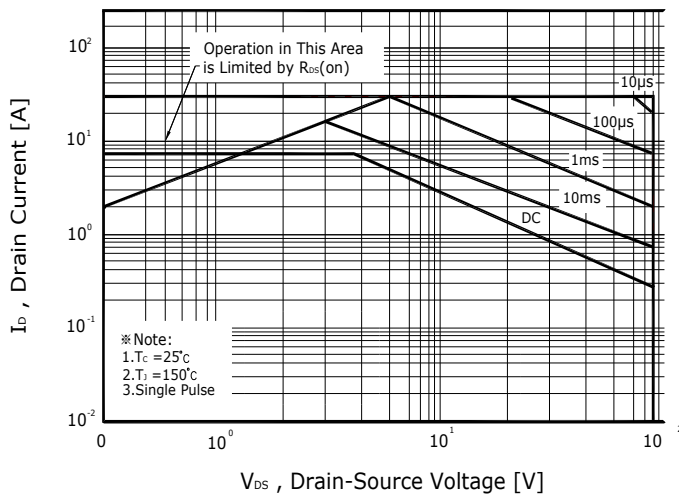


Fig. 10  $I_D - T_C$

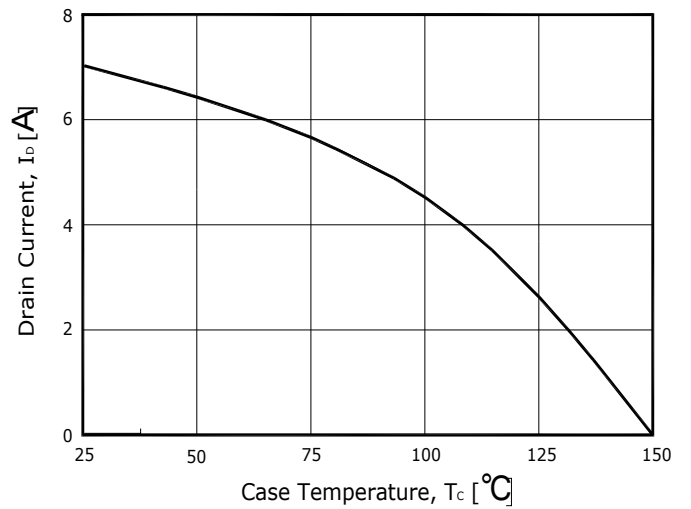


Fig. 11 Gate Charge Test Circuit & Waveform

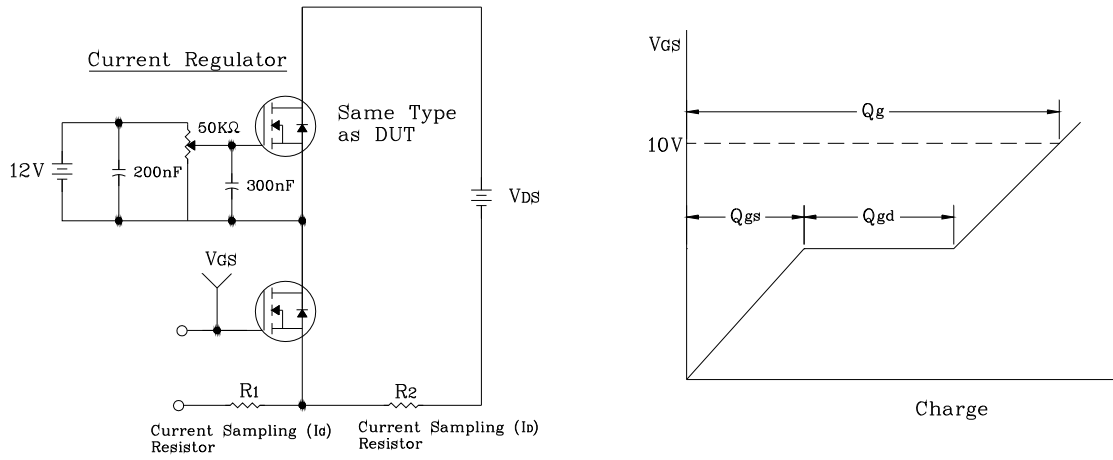


Fig. 12 Resistive Switching Test Circuit & Waveform

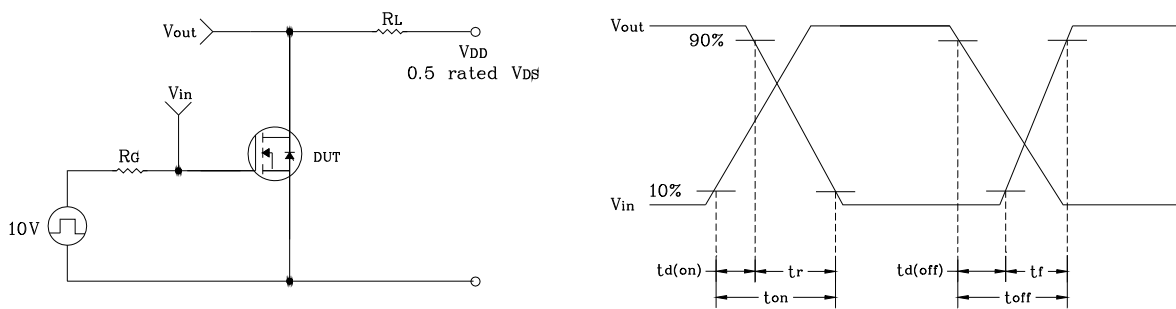


Fig. 13 EAS Test Circuit & Waveform

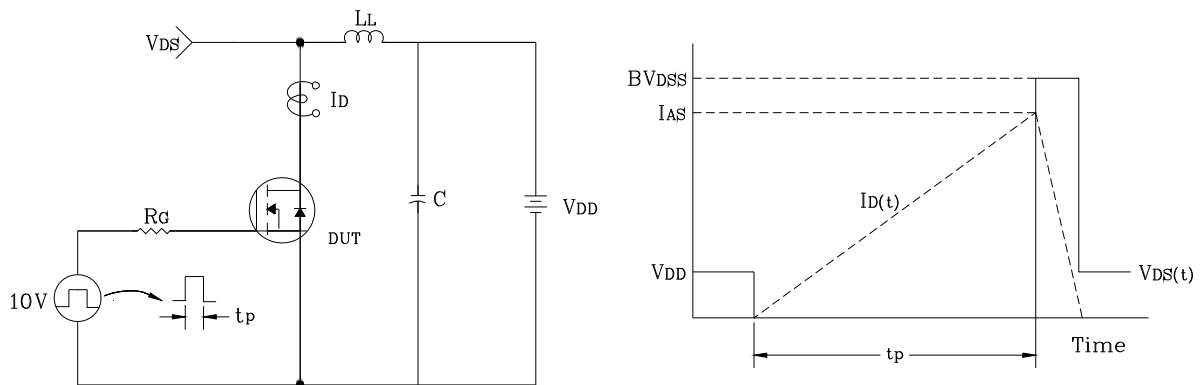
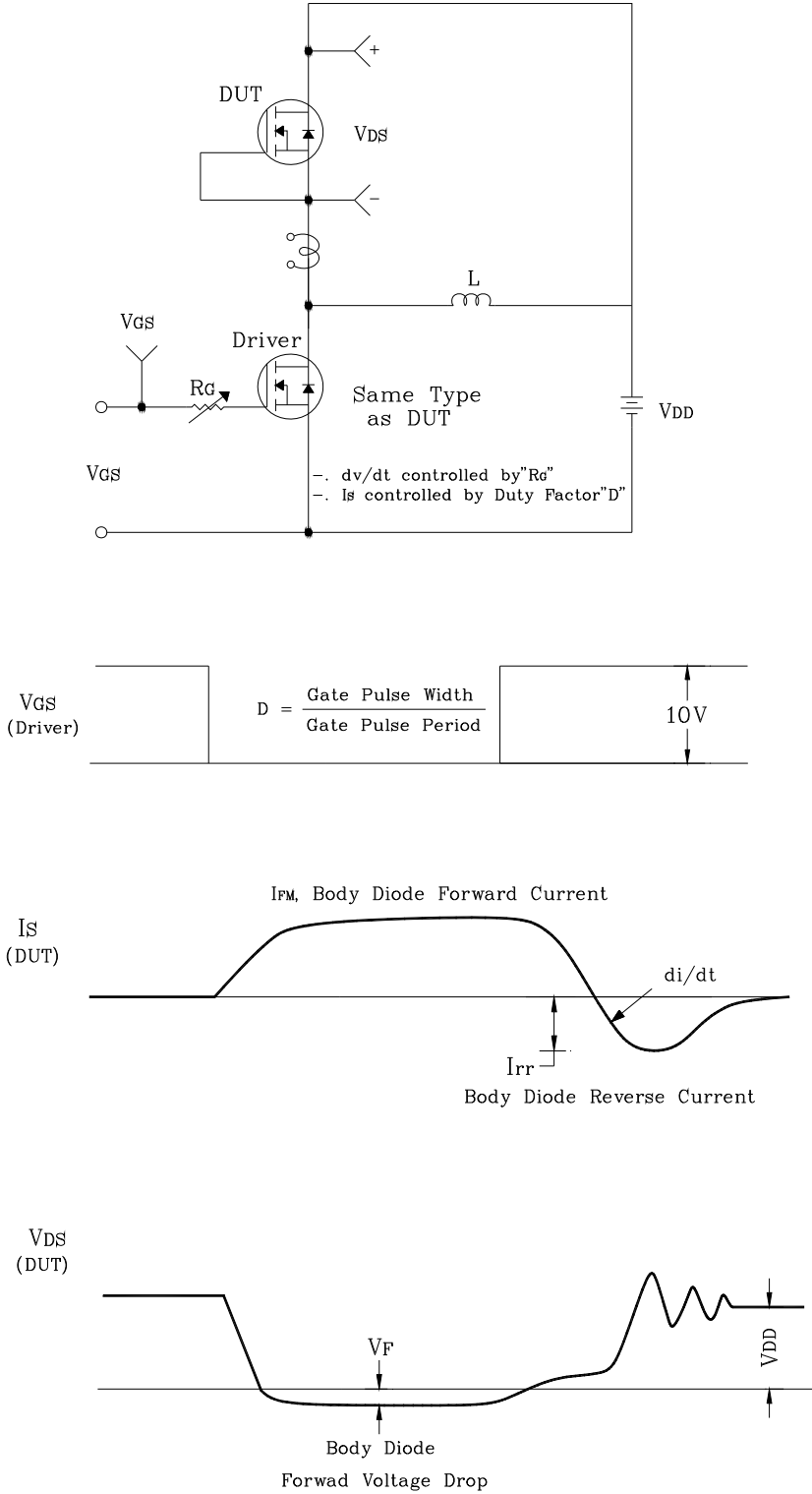


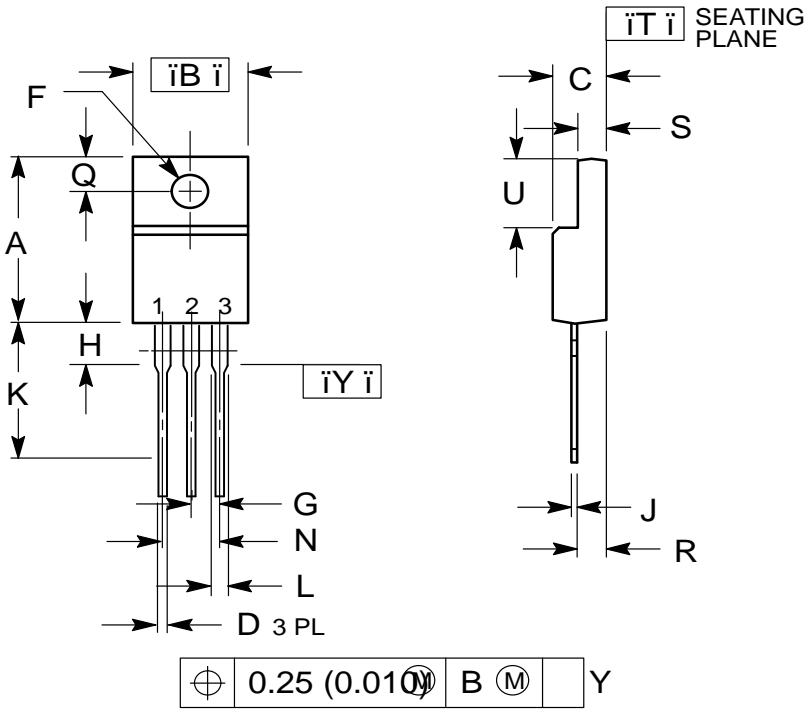
Fig. 14 Diode Reverse Recovery Time Test Circuit & Waveform



G  
Package Dimensions

G  
G

TO-220F



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH
  3. 221D-01 THRU 221D-02 OBSOLETE, NEW STANDARD 221D-03.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.617	0.635	15.67	16.12
B	0.392	0.419	9.96	10.63
C	0.177	0.193	4.50	4.90
D	0.024	0.039	0.60	1.00
F	0.116	0.129	2.95	3.28
G	0.100 BSC		2.54 BSC	
H	0.118	0.135	3.00	3.43
J	0.018	0.025	0.45	0.63
K	0.503	0.541	12.78	13.73
L	0.048	0.058	1.23	1.47
N	0.200 BSC		5.08 BSC	
Q	0.122	0.138	3.10	3.50
R	0.099	0.117	2.51	2.96
S	0.092	0.113	2.34	2.87
U	0.239	0.271	6.06	6.88