MAX 10 FPGA Device Datasheet

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This datasheet describes the electrical characteristics, switching characteristics, configuration specifications, and timing for MAX® 10 devices.

Table 1: MAX 10 Device Grades and Speed Grades Supported

Device Grade	Speed Grade Supported
Commercial	• –C7 • –C8 (slowest)
Industrial	• –I6 (fastest) • –I7
Automotive	–A7

Note: The –I6 speed grade MAX 10 FPGA device option is not available by default in the Quartus® II software. Contact your local Altera sales representatives for support.

Related Information

MAX 10 FPGA Device Overview

Provides more information about the densities and packages of devices in the MAX 10.

Electrical Characteristics

The following sections describe the operating conditions and power consumption of MAX 10 devices.

Operating Conditions

MAX 10 devices are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of the MAX 10 devices, you must consider the operating requirements described in this section.

Absolute Maximum Ratings

This section defines the maximum operating conditions for MAX 10 devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied for these conditions.

Caution: Conditions outside the range listed in the absolute maximum ratings tables may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

Single Supply Devices Absolute Maximum Ratings

Table 2: Absolute Maximum Ratings for MAX 10 Single Supply Devices—Preliminary

Symbol	Parameter	Min	Max	Unit
V_{CC_ONE}	Supply voltage for core and periphery through on-die voltage regulator	–0.5	3.9	V
V_{CCIO}	Supply voltage for input and output buffers	–0.5	3.9	V
V_{CCA}	Supply voltage for phase-locked loop (PLL) regulator and analog-to-digital converter (ADC) block (analog)	–0.5	3.9	V

Dual Supply Devices Absolute Maximum Ratings

Table 3: Absolute Maximum Ratings for MAX 10 Dual Supply Devices—Preliminary

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply voltage for core and periphery	–0.5	1.63	V
V_{CCIO}	Supply voltage for input and output buffers	–0.5	3.9	V
V_{CCA}	Supply voltage for PLL regulator (analog)	–0.5	3.41	V
V_{CCD_PLL}	Supply voltage for PLL regulator (digital)	–0.5	1.63	V

Symbol	Parameter	Min	Max	Unit
V_{CCA_ADC}	Supply voltage for ADC analog block	–0.5	3.41	V
V_{CCINT}	Supply voltage for ADC digital block	–0.5	1.63	V

Absolute Maximum Ratings

Table 4: Absolute Maximum Ratings for MAX 10 Devices—Preliminary

Symbol	Parameter	Min	Max	Unit
V_I	DC input voltage	–0.5	4.12	V
I_{OUT}	DC output current per pin	–25	25	mA
T_{STG}	Storage temperature	–65	150	°C
T_J	Operating junction temperature	–40	125	°C

Maximum Allowed Overshoot During Transitions over a 11.4-Year Time Frame

Table 5: Maximum Allowed Overshoot During Transitions over a 11.4-Year Time Frame for MAX 10 Devices

Condition (V)	Overshoot Duration as % of High Time	Unit
4.12	100.0	%
4.17	11.7	%
4.22	7.1	%
4.27	4.3	%
4.32	2.6	%
4.37	1.6	%
4.42	1.0	%
4.47	0.6	%
4.52	0.3	%

Condition (V)	Overshoot Duration as % of High Time	Unit
4.57	0.2	%

Recommended Operating Conditions

This section lists the functional operation limits for the AC and DC parameters for MAX 10 devices. The tables list the steady-state voltage values expected from MAX 10 devices. Power supply ramps must all be strictly monotonic, without plateaus.

Single Supply Devices Power Supplies Recommended Operating Conditions

Table 6: Power Supplies Recommended Operating Conditions for MAX 10 Single Supply Devices—Preliminary

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{CC_ONE} (1)	Supply voltage for core and periphery through on-die voltage regulator	—	2.85/3.135	3.0/3.3	3.15/3.465	V
V_{CCIO} (2)	Supply voltage for input and output buffers	3.3 V	3.135	3.3	3.465	V
		3.0 V	2.85	3	3.15	V
		2.5 V	2.375	2.5	2.625	V
		1.8 V	1.71	1.8	1.89	V
		1.5 V	1.425	1.5	1.575	V
		1.35 V	1.2825	1.35	1.4175	V
		1.2 V	1.14	1.2	1.26	V
V_{CCA} (1)	Supply voltage for PLL regulator and ADC block (analog)	—	2.85/3.135	3.0/3.3	3.15/3.465	V

(1) V_{CCA} must be connected to V_{CC_ONE} through a filter.
(2) V_{CCIO} for all I/O banks must be powered up during device operation.

Dual Supply Devices Power Supplies Recommended Operating Conditions

Table 7: Power Supplies Recommended Operating Conditions for MAX 10 Dual Supply Devices—Preliminary

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{CC}	Supply voltage for core and periphery	—	1.15	1.2	1.25	V
V_{CCIO} (3)	Supply voltage for input and output buffers	3.3 V	3.135	3.3	3.465	V
		3.0 V	2.85	3	3.15	V
		2.5 V	2.375	2.5	2.625	V
		1.8 V	1.71	1.8	1.89	V
		1.5 V	1.425	1.5	1.575	V
		1.35 V	1.2825	1.35	1.4175	V
		1.2 V	1.14	1.2	1.26	V
V_{CCA} (4)(5)	Supply voltage for PLL regulator (analog)	—	2.375	2.5	2.625	V
V_{CCD_PLL} (6)	Supply voltage for PLL regulator (digital)	—	1.15	1.2	1.25	V
V_{CCA_ADC}	Supply voltage for ADC analog block	—	2.375	2.5	2.625	V
V_{CCINT}	Supply voltage for ADC digital block	—	1.15	1.2	1.25	V

(3) V_{CCIO} for all I/O banks must be powered up during device operation.
(4) All V_{CCA} pins must be powered to 2.5 V (even when PLLs are not used), and must be powered up and powered down at the same time.
(5) All V_{CCA} pins must be connected together for EQFP package.
(6) V_{CCD_PLL} must always be connected to V_{CC} through a decoupling capacitor and ferrite bead.

Recommended Operating Conditions

Table 8: Recommended Operating Conditions for MAX 10 Devices—Preliminary

Symbol	Parameter	Condition	Min	Max	Unit
V_I	DC input voltage	—	–0.5	3.6	V
V_O	Output voltage for I/O pins	—	0	V_{CCIO}	V
T_J	Operating junction temperature	Commercial	0	85	°C
		Industrial	–40	100	°C
		Automotive	–40	125	°C
t_{RAMP}	Power supply ramp time	Standard POR(7)	200 µs	50 ms	—
		Fast POR (8)	200 µs	3 ms	—
		Instant-on	200 µs	3 ms	—
I_{Diode}	Magnitude of DC current across PCI clamp diode when enabled	—	—	10	mA

Programming/Erasure Specifications

Table 9: Programming/Erasure Specifications for MAX 10 Devices—Preliminary

Parameter	Block	Minimum	Unit
Erase and reprogram cycles	User flash memory (UFM) and Configuration flash memory (CFM)	10,000	Cycles
Data retention duration	UFM and CFM	10	Years

(7) Each individual power supply should reach the recommended operating range within 50 ms.
(8) Each individual power supply should reach the recommended operating range within 3 ms.

DC Characteristics

I/O Pin Leakage Current

The values in the table are specified for normal device operation. The values vary during device power-up. This applies for all V_{CCIO} settings (3.3, 3.0, 2.5, 1.8, 1.5, 1.35, and 1.2 V).

10 µA I/O leakage current limit is applicable when the internal clamping diode is off. A higher current can be the observed when the diode is on.

Table 10: I/O Pin Leakage Current for MAX 10 Devices—Preliminary

Symbol	Parameter	Condition	Min	Max	Unit
I_I	Input pin leakage current	V_I = 0 V to $V_{CCIOMAX}$	–10	10	µA
I_{OZ}	Tristated I/O pin leakage current	V_O = 0 V to $V_{CCIOMAX}$	–10	10	µA

Bus Hold Parameters

Bus hold retains the last valid logic state after the source driving it either enters the high impedance state or is removed. Each I/O pin has an option to enable bus hold in user mode. Bus hold is always disabled in configuration mode.

Table 11: Bus Hold Parameters for MAX 10 Devices—Preliminary

Parameter	Condition	V_{CCIO} (V)												Unit
		1.2		1.5		1.8		2.5		3		3.3		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Bus-hold low, sustaining current	$V_{IN} > V_{IL}$ (maximum)	8	—	12	—	30	—	50	—	70	—	70	—	µA
Bus-hold high, sustaining current	$V_{IN} < V_{IL}$ (minimum)	–8	—	–12	—	–30	—	–50	—	–70	—	–70	—	µA
Bus-hold low, overdrive current	0 V < V_{IN} < V_{CCIO}	—	125	—	175	—	200	—	300	—	500	—	500	µA
Bus-hold high, overdrive current	0 V < V_{IN} < V_{CCIO}	—	–125	—	–175	—	–200	—	–300	—	–500	—	–500	µA
Bus-hold trip point	—	0.3	0.9	0.375	1.125	0.68	1.07	0.7	1.7	0.8	2	0.8	2	V

Series OCT without Calibration Specifications

Table 12: Series OCT without Calibration Specifications for MAX 10 Devices—Preliminary

This table shows the variation of on-chip termination (OCT) without calibration across process, voltage, and temperature (PVT).

Description	V_{CCIO} (V)	Resistance Tolerance		Unit
		–C7, –I6, –I7, –A7	–C8	
Series OCT without calibration	3.00	±35	±30	%
	2.50	±35	±30	%
	1.80	±40	±35	%
	1.50	±40	±40	%
	1.35	±40	±50	%
	1.20	±45	±60	%

Series OCT with Calibration at Device Power-Up Specifications

Table 13: Series OCT with Calibration at Device Power-Up Specifications for MAX 10 Devices—Preliminary

OCT calibration is automatically performed at device power-up for OCT enabled I/Os.

Description	V_{CCIO} (V)	Calibration Accuracy	Unit
Series OCT with calibration at device power-up	3.00	±12	%
	2.50	±12	%
	1.80	±12	%
	1.50	±12	%
	1.35	±12	%
	1.20	±12	%

OCT Variation after Calibration at Device Power-Up

The OCT resistance may vary with the variation of temperature and voltage after calibration at device power-up.

Use the following table and equation to determine the final OCT resistance considering the variations after calibration at device power-up.

Table 14: OCT Variation after Calibration at Device Power-Up for MAX 10 Devices—Preliminary

This table lists the change percentage of the OCT resistance with voltage and temperature.

Desccription	Nominal Voltage	dR/dT (%/°C)	dR/dV (%/mV)
OCT variation after calibraiton at device power-up	3.00	0.25	–0.027
	2.50	0.245	–0.04
	1.80	0.242	–0.079
	1.50	0.235	–0.125
	1.35	0.229	–0.16
	1.20	0.197	–0.208

Figure 1: Equation for OCT Resistance after Calibration at Device Power-Up

$$\Delta R_V = (V_2 - V_1) \times 1000 \times dR/dV$$

$$\Delta R_T = (T_2 - T_1) \times dR/dT$$

$$\text{For } \Delta R_X < 0;\ MF_X = 1/(|\Delta R_X|/100 + 1)$$

$$\text{For } \Delta R_X > 0;\ MF_X = \Delta R_X/100 + 1$$

$$MF = MF_V \times MF_T$$

$$R_{final} = R_{initial} \times MF$$

The definitions for equation are as follows:

- T_1 is the initial temperature.
- T_2 is the final temperature.
- MF is multiplication factor.
- $R_{initial}$ is initial resistance.
- R_{final} is final resistance.
- Subscript x refers to both V and T.
- ΔR_V is variation of resistance with voltage.
- ΔR_T is variation of resistance with temperature.
- dR/dT is the change percentage of resistance with temperature after calibration at device power-up.
- dR/dV is the change percentage of resistance with voltage after calibration at device power-up.
- V_1 is the initial voltage.
- V_2 is final voltage.

The following figure shows the example to calculate the change of 50 Ω I/O impedance from 25°C at 3.0 V to 85°C at 3.15 V.

Figure 2: Example for OCT Resistance Calculation after Calibration at Device Power-Up

$$\Delta R_V = (3.15 - 3) \times 1000 \times -0.026 = -3.83$$

$$\Delta R_T = (85 - 25) \times 0.026 = 15.72$$

Because ΔR_V is negative,

$$MF_V = 1/(3.83/100 + 1) = 0.963$$

Because ΔR_T is positive,

$$MF_T = 15.72/100 + 1 = 1.157$$

$$MF = 0.963 \times 1.157 = 1.114$$

$$R_{final} = 50 \times 1.114 = 55.71\Omega$$

Pin Capacitance

Table 15: Pin Capacitance for MAX 10 Devices—Preliminary

Symbol	Parameter	Value	Unit
C_{IOB}	Input capacitance on bottom I/O pins	8	pF
C_{IOLRT}	Input capacitance on left/right/top I/O pins	7	pF
C_{LVDSB}	Input capacitance on bottom I/O pins with dedicated LVDS output (9)	8	pF
C_{ADCL}	Input capacitance on left I/O pins with ADC input (10)	9	pF
$C_{VREFLRT}$	Input capacitance on left/right/top dual purpose V_{REF} pin when used as V_{REF} or user I/O pin (11)	48	pF
C_{VREFB}	Input capacitance on bottom dual purpose V_{REF} pin when used as V_{REF} or user I/O pin	50	pF
C_{CLKB}	Input capacitance on bottom dual purpose clock input pins (12)	7	pF
C_{CLKLRT}	Input capacitance on left/right/top dual purpose clock input pins (12)	6	pF

Internal Weak Pull-Up Resistor

All I/O pins, except configuration, test, and JTAG pins, have an option to enable weak pull-up.

(9) Dedicated LVDS output buffer is only available at bottom I/O bank.
(10) ADC pins are only available at left I/O bank.
(11) When V_{REF} pin is used as regular input or output, F_{max} performance is reduced due to higher pin capacitance. Using the V_{REF} pin capacitance specification from device datasheet, perform SI analysis on your board setup to determine the F_{max} of your system.
(12) 10M40 and 10M50 devices have dual purpose clock input pins at top/bottom I/O banks.

Table 16: Internal Weak Pull-Up Resistor for MAX 10 Devices—Preliminary

Pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO}.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$R_{\_PU}$	Value of I/O pin pull-up resistor before and during configuration, as well as user mode if the programmable pull-up resistor option is enabled	V_{CCIO} = 3.3 V ± 5%	7	12	18	kΩ
		V_{CCIO} = 3.0 V ± 5%	8	13	20	kΩ
		V_{CCIO} = 2.5 V ± 5%	10	15	25	kΩ
		V_{CCIO} = 1.8 V ± 5%	16	25	46	kΩ
		V_{CCIO} = 1.5 V ± 5%	20	36	82	kΩ
		V_{CCIO} = 1.2 V ± 5%	33	82	175	kΩ

The internal weak pull-up resistor is defined in the following equation:

Figure 3: Internal Weak Pull-Up Resistor

$$R_{\_PU} = (V_{CCIO} - V_I)/I_{R\_PU}$$

Minimum condition: –40°C; $V_{CCIO} = V_{CC}$ + 5%; $V_I = V_{CC}$ + 5% – 50mV;

Typical condition: 25°C; $V_{CCIO} = V_{CC}$; V_I = 0 V;

Maximum condition: 125°C; $V_{CCIO} = V_{CC}$ – 5%; V_I = 0 V;

where V_I refers to the input voltage at the I/O pin.

Hot-Socketing Specifications

Table 17: Hot-Socketing Specifications for MAX 10 Devices—Preliminary

Symbol	Parameter	Maximum
$I_{IOPIN(DC)}$	DC current per I/O pin	300 µA

Symbol	Parameter	Maximum
$I_{IOPIN(AC)}$	AC current per I/O pin	8 mA (13)

Hysteresis Specifications for Schmitt Trigger Input

MAX 10 devices support Schmitt trigger input on all I/O pins. A Schmitt trigger feature introduces hysteresis to the input signal for improved noise immunity, especially for signal with slow edge rate.

Table 18: Hysteresis Specifications for Schmitt Trigger Input for MAX 10 Devices—Preliminary

Symbol	Parameter	Condition	Minimum	Unit
V_{HYS}	Hysteresis for Schmitt trigger input	V_{CCIO} = 3.3 V	180	mV
		V_{CCIO} = 2.5 V	150	mV
		V_{CCIO} = 1.8 V	120	mV
		V_{CCIO} = 1.5 V	110	mV

(13) The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, $|I_{IOPIN}| = C\ dv/dt$, in which C is I/O pin capacitance and dv/dt is the slew rate.

Figure 4: LVTTL/LVCMOS Input Standard Voltage Diagram

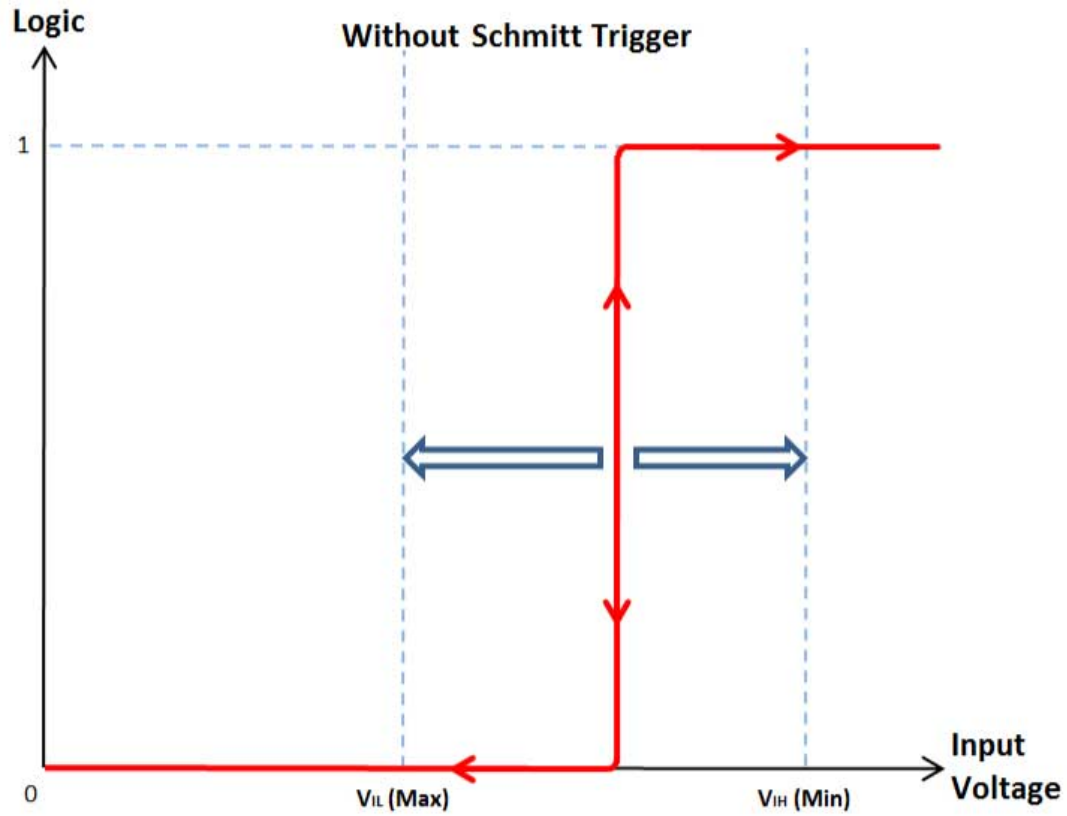
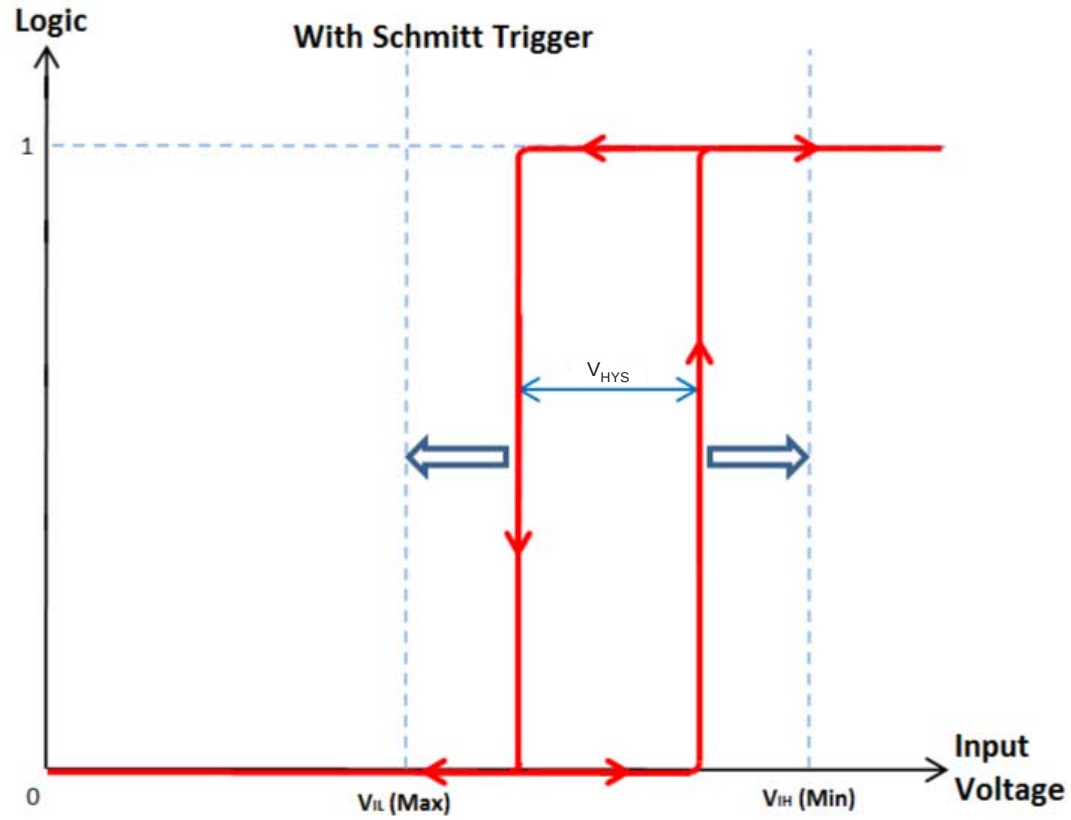


Figure 5: Schmitt Trigger Input Standard Voltage Diagram



I/O Standards Specifications

Tables in this section list input voltage (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for various I/O standards supported by MAX 10 devices.

For minimum voltage values, use the minimum V_{CCIO} values. For maximum voltage values, use the maximum V_{CCIO} values.

Single-Ended I/O Standards Specifications

Table 19: Single-Ended I/O Standards Specifications for MAX 10 Devices—Preliminary

To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the **3.3-V LVTTL** specification (4 mA), you should set the current strength settings to 4 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)	I_{OH} (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
3.3 V LVTTL	3.135	3.3	3.465	–0.3	0.8	1.7	3.6	0.45	2.4	4	–4
3.3 V LVCMOS	3.135	3.3	3.465	–0.3	0.8	1.7	3.6	0.2	V_{CCIO} – 0.2	2	–2
3.0 V LVTTL	2.85	3	3.15	–0.3	0.8	1.7	V_{CCIO} + 0.3	0.45	2.4	4	–4
3.0 V LVCMOS	2.85	3	3.15	–0.3	0.8	1.7	V_{CCIO} + 0.3	0.2	V_{CCIO} – 0.2	0.1	–0.1
2.5 V LVTTL and **LVCMOS**	2.375	2.5	2.625	–0.3	0.7	1.7	V_{CCIO} + 0.3	0.4	2	1	–1
1.8 V LVTTL and **LVCMOS**	1.71	1.8	1.89	–0.3	0.35 x V_{CCIO}	0.65 x V_{CCIO}	2.25	0.45	V_{CCIO} – 0.45	2	–2
1.5 V LVCMOS	1.425	1.5	1.575	–0.3	0.35 x V_{CCIO}	0.65 x V_{CCIO}	V_{CCIO} + 0.3	0.25 x V_{CCIO}	0.75 x V_{CCIO}	2	–2
1.2 V LVCMOS	1.14	1.2	1.26	–0.3	0.35 x V_{CCIO}	0.65 x V_{CCIO}	V_{CCIO} + 0.3	0.25 x V_{CCIO}	0.75 x V_{CCIO}	2	–2
3.3 V Schmitt Trigger	3.135	3.3	3.465	–0.3	0.8	1.7	V_{CCIO} + 0.3	—	—	—	—
2.5 V Schmitt Trigger	2.375	2.5	2.625	–0.3	0.7	1.7	V_{CCIO} + 0.3	—	—	—	—
1.8 V Schmitt Trigger	1.71	1.8	1.89	–0.3	0.35 x V_{CCIO}	0.65 x V_{CCIO}	V_{CCIO} + 0.3	—	—	—	—
1.5 V Schmitt Trigger	1.425	1.5	1.575	–0.3	0.35 x V_{CCIO}	0.65 x V_{CCIO}	V_{CCIO} + 0.3	—	—	—	—

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)	I_{OH} (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
3.0 V PCI	2.85	3	3.15	—	0.3 x V_{CCIO}	0.5 x V_{CCIO}	V_{CCIO} + 0.3	0.1 x V_{CCIO}	0.9 x V_{CCIO}	1.5	–0.5

Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications

Table 20: Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for MAX 10 Devices—Preliminary

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{TT} (V) (14)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	1.19	1.25	1.31	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04
SSTL-18 Class I, II	1.7	1.8	1.9	0.833	0.9	0.969	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04
SSTL-15 Class I, II	1.425	1.5	1.575	0.49 x V_{CCIO}	0.5 x V_{CCIO}	0.51 x V_{CCIO}	0.49 x V_{CCIO}	0.5 x V_{CCIO}	0.51 x V_{CCIO}
SSTL-135 Class I, II	1.283	1.35	1.45	0.49 x V_{CCIO}	0.5 x V_{CCIO}	0.51 x V_{CCIO}	0.49 x V_{CCIO}	0.5 x V_{CCIO}	0.51 x V_{CCIO}
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	0.85	0.9	0.95
HSTL-15 Class I, II	1.425	1.5	1.575	0.71	0.75	0.79	0.71	0.75	0.79
HSTL-12 Class I, II	1.14	1.2	1.26	0.48 x V_{CCIO} (15)	0.5 x V_{CCIO} (15)	0.52 x V_{CCIO} (15)	—	0.5 x V_{CCIO}	—
				0.47 x V_{CCIO} (16)	0.5 x V_{CCIO} (16)	0.53 x V_{CCIO} (16)			

(14) V_{TT} of transmitting device must track V_{REF} of the receiving device.
(15) Value shown refers to DC input reference voltage, $V_{REF(DC)}$.
(16) Value shown refers to AC input reference voltage, $V_{REF(AC)}$.

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{TT} (V) [14]		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
HSUL-12	1.14	1.2	1.3	0.49 x V_{CCIO}	0.5 x V_{CCIO}	0.51 x V_{CCIO}	—	—	—

Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications

Table 21: Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for MAX 10 Devices—Preliminary

To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the **SSTL-15 Class I** specification (8 mA), you should set the current strength settings to 8 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)		$V_{IH(AC)}$ (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)	I_{OH} (mA)
	Min	Max	Min	Max	Min	Max	Min	Max	Max	Min		
SSTL-2 Class I	—	V_{REF} – 0.18	V_{REF} + 0.18	—	—	V_{REF} – 0.35	V_{REF} + 0.35	—	V_{TT} – 0.57	V_{TT} + 0.57	8.1	–8.1
SSTL-2 Class II	—	V_{REF} – 0.18	V_{REF} + 0.18	—	—	V_{REF} – 0.35	V_{REF} + 0.35	—	V_{TT} – 0.76	V_{TT} + 0.76	16.4	–16.4
SSTL-18 Class I	—	V_{REF} – 0.125	V_{REF} + 0.125	—	—	V_{REF} – 0.25	V_{REF} + 0.25	—	V_{TT} – 0.475	V_{TT} + 0.475	6.7	–6.7
SSTL-18 Class II	—	V_{REF} – 0.125	V_{REF} + 0.125	—	—	V_{REF} – 0.25	V_{REF} + 0.25	—	0.28	V_{CCIO} – 0.28	13.4	–13.4
SSTL-15 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	—	V_{REF} – 0.175	V_{REF} + 0.175	—	0.2 x V_{CCIO}	0.8 x V_{CCIO}	8	–8
SSTL-15 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	—	V_{REF} – 0.175	V_{REF} + 0.175	—	0.2 x V_{CCIO}	0.8 x V_{CCIO}	16	–16
SSTL-135	—	V_{REF} – 0.09	V_{REF} + 0.09	—	—	V_{REF} – 0.16	V_{REF} + 0.16	—	0.2 x V_{CCIO}	0.8 x V_{CCIO}	—	—
HSTL-18 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	—	V_{REF} – 0.2	V_{REF} + 0.2	—	0.4	V_{CCIO} – 0.4	8	–8

[14] V_{TT} of transmitting device must track V_{REF} of the receiving device.

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)		$V_{IH(AC)}$ (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)	I_{OH} (mA)
	Min	Max	Min	Max	Min	Max	Min	Max	Max	Min		
HSTL-18 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	—	V_{REF} – 0.2	V_{REF} + 0.2	—	0.4	V_{CCIO} – 0.4	16	–16
HSTL-15 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	—	V_{REF} – 0.2	V_{REF} + 0.2	—	0.4	V_{CCIO} – 0.4	8	–8
HSTL-15 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	—	V_{REF} – 0.2	V_{REF} + 0.2	—	0.4	V_{CCIO} – 0.4	16	–16
HSTL-12 Class I	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	–0.24	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCIO} + 0.24	0.25 x V_{CCIO}	0.75 x V_{CCIO}	8	–8
HSTL-12 Class II	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	–0.24	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCIO} + 0.24	0.25 x V_{CCIO}	0.75 x V_{CCIO}	14	–14
HSUL-12	—	V_{REF} – 0.13	V_{REF} + 0.13	—	—	V_{REF} – 0.22	V_{REF} + 0.22	—	0.1 x V_{CCIO}	0.9 x V_{CCIO}	—	—

Differential SSTL I/O Standards Specifications

Differential SSTL requires a V_{REF} input.

Table 22: Differential SSTL I/O Standards Specifications for MAX 10 Devices—Preliminary

I/O Standard	V_{CCIO} (V)			$V_{Swing(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{Swing(AC)}$ (V)	
	Min	Typ	Max	Min	Max[17]	Min	Typ	Max	Min	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.36	V_{CCIO}	$V_{CCIO}/2$ – 0.2	—	$V_{CCIO}/2$+ 0.2	0.7	V_{CCIO}
SSTL-18 Class I, II	1.7	1.8	1.9	0.25	V_{CCIO}	$V_{CCIO}/2$ – 0.175	—	$V_{CCIO}/2$+ 0.175	0.5	V_{CCIO}
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	$V_{CCIO}/2$ – 0.15	—	$V_{CCIO}/2$ + 0.15	$2(V_{IH(AC)} – V_{REF})$	$2(V_{IL(AC)} – V_{REF})$

(17) The maximum value for $V_{SWING(DC)}$ is not defined. However, each single-ended signal needs to be within the respective single-ended limits ($V_{IH(DC)}$ and $V_{IL(DC)}$).

I/O Standard	V_{CCIO} (V)			$V_{Swing(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{Swing(AC)}$ (V)	
	Min	Typ	Max	Min	Max[17]	Min	Typ	Max	Min	Max
SSTL-135	1.283	1.35	1.45	0.18	—	V_{REF} – 0.135	0.5 x V_{CCIO}	V_{REF} + 0.135	$2(V_{IH(AC)} - V_{REF})$	$2(V_{IL(AC)} - V_{REF})$

Differential HSTL and HSUL I/O Standards Specifications

Differential HSTL requires a V_{REF} input.

Table 23: Differential HSTL and HSUL I/O Standards Specifications for MAX 10 Devices—Preliminary

I/O Standard	V_{CCIO} (V)			$V_{DIF(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{CM(DC)}$ (V)			$V_{DIF(AC)}$ (V)
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	—	0.85	—	0.95	0.85	—	0.95	0.4
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.71	—	0.79	0.71	—	0.79	0.4
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	V_{CCIO}	0.48 x V_{CCIO}	0.5 x V_{CCIO}	0.52 x V_{CCIO}	0.48 x V_{CCIO}	0.5 x V_{CCIO}	0.52 x V_{CCIO}	0.3
HSUL-12	1.14	1.2	1.3	0.26	—	0.5 x V_{CCIO} – 0.12	0.5 x V_{CCIO}	0.5 x V_{CCIO} + 0.12	0.4 x V_{CCIO}	0.5 x V_{CCIO}	0.6 x V_{CCIO}	0.44

(17) The maximum value for $V_{SWING(DC)}$ is not defined. However, each single-ended signal needs to be within the respective single-ended limits ($V_{IH(DC)}$ and $V_{IL(DC)}$).

Differential I/O Standards Specifications

Table 24: Differential I/O Standards Specifications for MAX 10 Devices—Preliminary

I/O Standard	V_{CCIO} (V)			V_{ID} (mV)		V_{ICM} (V) (18)			V_{OD} (mV) (19)(20)			V_{OS} (V) (19)		
	Min	Typ	Max	Min	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
LVPECL (21)	2.375	2.5	2.625	100	—	0.05	D_{MAX} ≤ 500 Mbps	1.8	—	—	—	—	—	—
						0.55	500 Mbps ≤ D_{MAX} ≤ 700 Mbps	1.8						
						1.05	D_{MAX} > 700 Mbps	1.55						
LVDS	2.375	2.5	2.625	100	—	0.05	D_{MAX} ≤ 500 Mbps	1.8	247	—	600	1.125	1.25	1.375
						0.55	500 Mbps ≤ D_{MAX} ≤ 700 Mbps	1.8						
						1.05	D_{MAX} > 700 Mbps	1.55						
BLVDS (22)	2.375	2.5	2.625	100	—	—	—	—	—	—	—	—	—	—
mini-LVDS (23)	2.375	2.5	2.625	—	—	—	—	—	300	—	600	1	1.2	1.4
RSDS (23)	2.375	2.5	2.625	—	—	—	—	—	100	200	600	0.5	1.2	1.5
PPDS (Row I/Os) (23)	2.375	2.5	2.625	—	—	—	—	—	100	200	600	0.5	1.2	1.4

(18) V_{IN} range: 0 V ≤ V_{IN} ≤ 1.85 V.
(19) R_L range: 90 ≤ R_L ≤ 110 Ω.
(20) Low V_{OD} setting is only supported for **RSDS** standard.
(21) **LVPECL** input standard is only supported at clock input. Output standard is not supported.
(22) No fixed V_{IN} , V_{OD} , and V_{OS} specifications for Bus LVDS (**BLVDS**). They are dependent on the system topology.
(23) **Mini-LVDS**, **RSDS**, and Point-to-Point Differential Signaling (**PPDS**) standards are only supported at the output pins for MAX 10 devices.

I/O Standard	V_{CCIO} (V)			V_{ID} (mV)		V_{ICM} (V) [18]			V_{OD} (mV) [19][20]			V_{OS} (V) [19]		
	Min	Typ	Max	Min	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
TMDS[24]	2.375	2.5	2.625	100	—	0.05	$D_{MAX} \leq$ 500 Mbps	1.8	—	—	—	—	—	—
						0.55	500 Mbps $\leq D_{MAX} \leq$ 700 Mbps	1.8						
						1.05	D_{MAX} > 700 Mbps	1.55						
Sub-LVDS [25]	1.71	1.8	1.89	100	—	0.55	—	1.25	[26]			0.8	0.9	1
SLVS	2.375	2.5	2.625	100	—	0.05	—	1.1	[26]			[27]		
HiSpi	2.375	2.5	2.625	100	—	0.05	$D_{MAX} \leq$ 500 Mbps	1.8	—	—	—	—	—	—
						0.55	500 Mbps $\leq D_{MAX} \leq$ 700 Mbps	1.8						
						1.05	D_{MAX} > 700 Mbps	1.55						

Switching Characteristics

This section provides the performance characteristics of MAX 10 core and periphery blocks.

[18] V_{IN} range: 0 V ≤ V_{IN} ≤ 1.85 V.
[19] R_L range: 90 ≤ R_L ≤ 110 Ω.
[20] Low V_{OD} setting is only supported for **RSDS** standard.
[24] Supported with requirement of an external level shift
[25] **Sub-LVDS** input buffer is using 2.5 V differential buffer.
[26] Differential output depends on the values of the external termination resistors.
[27] Differential output offset voltage depends on the values of the external termination resistors.

Core Performance Specifications

Clock Tree Specifications

Table 25: Clock Tree Specifications for MAX 10 Devices—Preliminary

Device	Performance					Unit
	–I6	–C7	–I7	–A7	–C8	
10M02	450	416	416	382	402	MHz
10M04	450	416	416	382	402	MHz
10M08	450	416	416	382	402	MHz
10M16	450	416	416	382	402	MHz
10M25	450	416	416	382	402	MHz
10M40	450	416	416	382	402	MHz
10M50	450	416	416	382	402	MHz

PLL Specifications

Table 26: PLL Specifications for MAX 10 Devices—Preliminary

V_{CCD_PLL} should always be connected to V_{CCINT} through decoupling capacitor and ferrite bead.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{IN} (28)	Input clock frequency	—	5	—	472.5	MHz
f_{INPFD}	Phase frequency detector (PFD) input frequency	—	5	—	325	MHz
f_{VCO} (29)	PLL internal voltage-controlled oscillator (VCO) operating range	—	600	—	1300	MHz

(28) This parameter is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.
(29) The VCO frequency reported by the Quartus II software in the PLL summary section of the compilation report takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the f_{VCO} specification.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{INDUTY}	Input clock duty cycle	—	40	—	60	%
$t_{INJITTER\_CCJ}$ (30)	Input clock cycle-to-cycle jitter	$F_{INPFD} \geq 100$ MHz	—	—	0.15	UI
		$F_{INPFD} < 100$ MHz	—	—	750	ps
f_{OUT_EXT} (28)	PLL output frequency for external clock output	—	—	—	472.5	MHz
f_{OUT}	PLL output frequency to global clock	–6 speed grade	—	—	472.5	MHz
		–7 speed grade	—	—	450	MHz
		–8 speed grade	—	—	402.5	MHz
$t_{OUTDUTY}$	Duty cycle for external clock output	Duty cycle set to 50%	45	50	55	%
t_{LOCK}	Time required to lock from end of device configuration	—	—	—	1	ms
t_{DLOCK}	Time required to lock dynamically	After switchover, reconfiguring any non-post-scale counters or delays, or when `areset` is deasserted	—	—	1	ms
$t_{OUTJITTER\_PERIOD\_IO}$ (31)	Regular I/O period jitter	$F_{OUT} \geq 100$ MHz	—	—	650	ps
		$F_{OUT} < 100$ MHz	—	—	75	mUI
$t_{OUTJITTER\_CCJ\_IO}$ (31)	Regular I/O cycle-to-cycle jitter	$F_{OUT} \geq 100$ MHz	—	—	60	ps
		$F_{OUT} < 100$ MHz	—	—	75	mUI
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	—	±50	ps
t_{ARESET}	Minimum pulse width on areset signal.	—	10	—	—	ns

(30) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source, which is less than 200 ps.

(31) Peak-to-peak jitter with a probability level of 10^{-12} (14 sigma, 99.99999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$t_{CONFIGPLL}$	Time required to reconfigure scan chains for PLLs	—	—	3.5 (32)	—	SCANCLK cycles
$f_{SCANCLK}$	scanclk frequency	—	—	—	100	MHz

Table 27: PLL Specifications for MAX 10 Single Supply Devices—Preliminary

Symbol	Parameter	Condition	Max	Unit
$t_{OUTJITTER\_PERIOD\_DEDCLK}$ (31)	Dedicated clock output period jitter	$F_{OUT} \geq 100$ MHz	660	ps
		$F_{OUT} < 100$ MHz	66	mUI
$t_{OUTJITTER\_CCJ\_DEDCLK}$ (31)	Dedicated clock output cycle-to-cycle jitter	$F_{OUT} \geq 100$ MHz	660	ps
		$F_{OUT} < 100$ MHz	66	mUI

Table 28: PLL Specifications for MAX 10 Dual Supply Devices—Preliminary

Symbol	Parameter	Condition	Max	Unit
$t_{OUTJITTER\_PERIOD\_DEDCLK}$ (31)	Dedicated clock output period jitter	$F_{OUT} \geq 100$ MHz	300	ps
		$F_{OUT} < 100$ MHz	30	mUI
$t_{OUTJITTER\_CCJ\_DEDCLK}$ (31)	Dedicated clock output cycle-to-cycle jitter	$F_{OUT} \geq 100$ MHz	300	ps
		$F_{OUT} < 100$ MHz	30	mUI

(32) With 100 MHz scanclk frequency.

Embedded Multiplier Specifications

Table 29: Embedded Multiplier Specifications for MAX 10 Devices—Preliminary

Mode	Number of Multipliers	Power Supply Mode	Performance			Unit
			–I6	–C7, –I7, –A7	–C8	
9 x 9-bit multiplier	1	Single supply mode	198	183	160	MHz
		Dual supply mode	234	212	180	MHz
18 x 18-bit multiplier	1	Single supply mode	198	183	160	MHz
		Dual supply mode	234	212	180	MHz

Memory Block Performance Specifications

Table 30: Memory Block Performance Specifications for MAX 10 Devices—Preliminary

Memory	Mode	Resources Used		Power Supply Mode	Performance			Unit
		LEs	M9K Memory		–I6	–C7, –I7, –A7	–C8	
M9K Block	FIFO 256 x 36	47	1	Single supply mode	232	219	204	MHz
				Dual supply mode	284	260	238	MHz
	Single-port 256 x 36	0	1	Single supply mode	232	219	204	MHz
				Dual supply mode	284	260	238	MHz
	Simple dual-port 256 x 36 CLK	0	1	Single supply mode	232	219	204	MHz
				Dual supply mode	284	260	238	MHz
	True dual port 512 x 18 single CLK	0	1	Single supply mode	232	219	204	MHz
				Dual supply mode	284	260	238	MHz

UFM Performance Specifications

Table 31: UFM Performance Specifications for MAX 10 Devices—Preliminary

Block	Mode	Performance	Unit
		–I6, –C7, –I7, –A7, –C8	
UFM	Avalon-MM slave	116	MHz

ADC Performance Specifications

Single Supply Devices ADC Performance Specifications

Table 32: ADC Performance Specifications for MAX 10 Single Supply Devices—Preliminary

Parameter	Symbol	Condition	Min	Typ	Max	Unit
ADC resolution	—	—	—	—	12	bits
ADC supply voltage	V_{CC_ONE}	—	2.85	3.0/3.3	3.465	V
External reference voltage	V_{REF}	—	V_{CC_ONE} – 0.5	—	V_{CC_ONE}	V
Sampling rate	F_S	Accumulative sampling rate	—	—	1000	kSPS
Input frequency	F_{IN}	—	—	—	50	kHz
Operating ambient temperature range	T_A	—	–40	25	125	°C
Analog input voltage	V_{IN}	Prescalar disabled	0	—	V_{REF}	V
		Prescalar enabled	0	—	3.6	V
Input resistance	R_{IN}	—	—	(33)	—	kΩ
Input capcitance	C_{IN}	Dedicated analog input	—	(33)	—	pF
		Dual function pin	—	(33)	—	pF

(33) Refer to the MAX 10 Analog-to-Digital Converter User Guide for the RC equation.

Parameter		Symbol	Condition	Min	Typ	Max	Unit
DC Accuracy	Offset error and drift	E_{offset}	Prescalar disabled	–0.2	—	0.2	%FS
			Prescalar enabled	–0.5	—	0.5	%FS
	Gain error and drift	E_{gain}	Prescalar disabled	–0.5	—	0.5	%FS
			Prescalar enabled	–0.75	—	0.75	%FS
	Differential non linearity	DNL	No missing codes	–0.9	—	0.9	LSB
	Integral non linearity	INL	—	–2	—	2	LSB
AC Accuracy	Total harmonic distortion	THD	F_{IN} = 50 kHz, F_S = 1 MHz, PLL	65	—	—	dB
	Signal-to-noise ratio	SNR	F_{IN} = 50 kHz, F_S = 1 MHz, PLL	54	—	—	dB
	Signal-to-noise and distortion	SINAD	F_{IN} = 50 kHz, F_S = 1 MHz, PLL	53	—	—	dB
On-Chip Temperature Sensor	Temperature sampling rate	T_S	—	—	—	50	kSPS
	Absolute accuracy	—	–40 to 125°C	—	—	±10	°C
Conversion Rate (34)	Conversion time	—	Single measurement	—	—	1	Cycle
			Continuous measurement	—	—	1	Cycle
			Temperature measurement	—	—	1	Cycle

Related Information

MAX 10 Analog-to-Digital Converter User Guide

Provides more information about the conversion rate and RC equation.

(34) For more detailed description, refer to Timing section in the MAX 10 Analog-to-Digital Converter User Guide.

Dual Supply Devices ADC Performance Specifications

Table 33: ADC Performance Specifications for MAX 10 Dual Supply Devices—Preliminary

Parameter	Symbol	Condition	Min	Typ	Max	Unit
ADC resolution	—	—	—	—	12	bits
Analog supply voltage	V_{CCA_ADC}	—	2.375	2.5	2.625	V
Digital supply voltage	V_{CCINT}	—	1.14	1.2	1.26	V
External reference voltage	V_{REF}	—	V_{CCA_ADC} – 0.5	—	V_{CCA_ADC}	V
Sampling rate	F_S	Accumulative sampling rate	—	—	1000	kSPS
Input frequency	F_{IN}	—	—	—	50	kHz
Operating ambient temperature range	T_A	—	–40	25	125	°C
Analog input voltage	V_{IN}	Prescalar disabled	0	—	V_{REF}	V
		Prescalar enabled	0	—	3	V
Analog supply current (DC)	I_{ACC_ADC}	Average current	—	275	450	µA
Digital supply current (DC)	I_{CCINT}	Average current	—	65	150	µA
Input resistance	R_{IN}	—	—	(35)	—	kΩ
Input capcitance	C_{IN}	Dedicated analog input	—	(35)	—	pF
		Dual function pin	—	(35)	—	pF

(35) Refer to the MAX 10 Analog-to-Digital Converter User Guide for the RC equation.

Parameter		Symbol	Condition	Min	Typ	Max	Unit
DC Accuracy	Offset error and drift	E_{offset}	Prescalar disabled	–0.2	—	0.2	%FS
			Prescalar enabled	–0.5	—	0.5	%FS
	Gain error and drift	E_{gain}	Prescalar disabled	–0.5	—	0.5	%FS
			Prescalar enabled	–0.75	—	0.75	%FS
	Differential non linearity	DNL	No missing codes	–0.9	—	0.9	LSB
	Integral non linearity	INL	—	–2	—	2	LSB
AC Accuracy	Total harmonic distortion	THD	F_{IN} = 50 kHz, F_S = 1 MHz, PLL	70 (36)	—	—	dB
	Signal-to-noise ratio	SNR	F_{IN} = 50 kHz, F_S = 1 MHz, PLL	62 (37)	—	—	dB
	Signal-to-noise and distortion	SINAD	F_{IN} = 50 kHz, F_S = 1 MHz, PLL	61.5 (38)	—	—	dB
On-Chip Temperature Sensor	Temperature sampling rate	T_S	—	—	—	50	kSPS
	Absolute accuracy	—	–40 to 125°C	—	—	±5	°C
Conversion Rate (39)	Conversion time	—	Single measurement	—	—	1	Cycle
			Continuous measurement	—	—	1	Cycle
			Temperature measurement	—	—	1	Cycle

Related Information

MAX 10 Analog-to-Digital Converter User Guide

Provides more information about the conversion rate and RC equation.

(36) Total harmonic distortion is 65 dB for dual function pin.
(37) Signal-to-noise ratio is 54 dB for dual function pin.
(38) Signal-to-noise and distortion is 53 dB for dual function pin.
(39) For more detailed description, refer to Timing section in the MAX 10 Analog-to-Digital Converter User Guide.

Periphery Performance Specifications

This section describes the periphery performance, high-speed I/O, and external memory interface.

Actual achievable frequency depends on design and system specific factors. Perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

High-Speed I/O Specifications

For more information about the high-speed and low-speed I/O performance pins, refer to the respective device pin-out files.

True PPDS and Emulated PPDS_E_3R Transmitter Timing Specifications

Table 34: True PPDS and Emulated PPDS_E_3R Transmitter Timing Specifications for MAX 10 Dual Supply Devices—Preliminary

True **PPDS** transmitter is only supported at bottom I/O bank. Emulated **PPDS** transmitter is supported at the output pin of all I/O banks.

Symbol	Parameter	Mode	–I6, –C7, –I7			–A7			–C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK}	Input clock frequency (high-speed I/O performance pin)	x10	5	—	155	5	—	150	5	—	155	MHz
		x8	5	—	155	5	—	150	5	—	155	MHz
		x7	5	—	155	5	—	150	5	—	155	MHz
		x4	5	—	155	5	—	150	5	—	155	MHz
		x2	5	—	155	5	—	150	5	—	155	MHz
		x1	5	—	310	5	—	300	5	—	310	MHz
HSIODR	Data rate (high-speed I/O performance pin)	x10	100	—	310	100	—	300	100	—	310	Mbps
		x8	80	—	310	80	—	300	80	—	310	Mbps
		x7	70	—	310	70	—	300	70	—	310	Mbps
		x4	40	—	310	40	—	300	40	—	310	Mbps
		x2	20	—	310	20	—	300	20	—	310	Mbps
		x1	10	—	310	10	—	300	10	—	310	Mbps

Symbol	Parameter	Mode	–I6, –C7, –I7			–A7			–C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK}	Input clock frequency (low-speed I/O performance pin)	x10	5	—	150	5	—	145	5	—	150	MHz
		x8	5	—	150	5	—	145	5	—	150	MHz
		x7	5	—	150	5	—	145	5	—	150	MHz
		x4	5	—	150	5	—	145	5	—	150	MHz
		x2	5	—	150	5	—	145	5	—	150	MHz
		x1	5	—	300	5	—	290	5	—	300	MHz
HSIODR	Data rate (low-speed I/O performance pin)	x10	100	—	300	100	—	290	100	—	300	Mbps
		x8	80	—	300	80	—	290	80	—	300	Mbps
		x7	70	—	300	70	—	290	70	—	300	Mbps
		x4	40	—	300	40	—	290	40	—	300	Mbps
		x2	20	—	300	20	—	290	20	—	300	Mbps
		x1	10	—	300	10	—	290	10	—	300	Mbps
t_{DUTY}	Duty cycle on transmitter output clock	—	45	—	55	45	—	55	45	—	55	%
TCCS[40]	Transmitter channel-to-channel skew	—	—	—	340	—	—	340	—	—	340	ps
$t_{x\ Jitter}$	Output jitter	—	—	—	500	—	—	500	—	—	500	ps
t_{RISE}	Rise time	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t_{FALL}	Fall time	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps

(40) TCCS specifications apply to I/O banks from the same side only.

Symbol	Parameter	Mode	–I6, –C7, –I7			–A7			–C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{LOCK}	Time required for the PLL to lock from the end of device configuration.	—	—	—	1	—	—	1	—	—	1	ms

True RSDS and Emulated RSDS_E_3R Transmitter Timing Specifications

Table 35: True RSDS and Emulated RSDS_E_3R Transmitter Timing Specifications for MAX 10 Dual Supply Devices—Preliminary

True **RSDS** transmitter is only supported at bottom I/O bank. Emulated **RSDS** transmitter is supported at the output pin of all I/O banks.

Symbol	Parameter	Mode	–I6, –C7, –I7			–A7			–C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK}	Input clock frequency (high-speed I/O performance pin)	x10	5	—	155	5	—	150	5	—	155	MHz
		x8	5	—	155	5	—	150	5	—	155	MHz
		x7	5	—	155	5	—	150	5	—	155	MHz
		x4	5	—	155	5	—	150	5	—	155	MHz
		x2	5	—	155	5	—	150	5	—	155	MHz
		x1	5	—	310	5	—	300	5	—	310	MHz
HSIODR	Data rate (high-speed I/O performance pin)	x10	100	—	310	100	—	300	100	—	310	Mbps
		x8	80	—	310	80	—	300	80	—	310	Mbps
		x7	70	—	310	70	—	300	70	—	310	Mbps
		x4	40	—	310	40	—	300	40	—	310	Mbps
		x2	20	—	310	20	—	300	20	—	310	Mbps
		x1	10	—	310	10	—	300	10	—	310	Mbps

Symbol	Parameter	Mode	–I6, –C7, –I7			–A7			–C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK}	Input clock frequency (low-speed I/O performance pin)	x10	5	—	150	5	—	145	5	—	150	MHz
		x8	5	—	150	5	—	145	5	—	150	MHz
		x7	5	—	150	5	—	145	5	—	150	MHz
		x4	5	—	150	5	—	145	5	—	150	MHz
		x2	5	—	150	5	—	145	5	—	150	MHz
		x1	5	—	300	5	—	290	5	—	300	MHz
HSIODR	Data rate (low-speed I/O performance pin)	x10	100	—	300	100	—	290	100	—	300	Mbps
		x8	80	—	300	80	—	290	80	—	300	Mbps
		x7	70	—	300	70	—	290	70	—	300	Mbps
		x4	40	—	300	40	—	290	40	—	300	Mbps
		x2	20	—	300	20	—	290	20	—	300	Mbps
		x1	10	—	300	10	—	290	10	—	300	Mbps
t_{DUTY}	Duty cycle on transmitter output clock	—	45	—	55	45	—	55	45	—	55	%
TCCS[41]	Transmitter channel-to-channel skew	—	—	—	340	—	—	340	—	—	340	ps
$t_{x\ Jitter}$	Output jitter (for multi supply devices)	—	—	—	500	—	—	500	—	—	500	ps
t_{RISE}	Rise time	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps

(41) TCCS specifications apply to I/O banks from the same side only.

Symbol	Parameter	Mode	–I6, –C7, –I7			–A7			–C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{FALL}	Fall time	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t_{LOCK}	Time required for the PLL to lock from the end of device configuration.	—	—	—	1	—	—	1	—	—	1	ms

Emulated RSDS_E_1R Transmitter Timing Specifications

Table 36: Emulated RSDS_E_1R Transmitter Timing Specifications for MAX 10 Dual Supply Devices—Preliminary

Emulated **RSDS_E_1R** transmitter is supported at the output pin of all I/O banks.

Symbol	Parameter	Mode	–I6, –C7, –I7			–A7			–C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK}	Input clock frequency (high-speed I/O performance pin)	x10	5	—	85	5	—	85	5	—	85	MHz
		x8	5	—	85	5	—	85	5	—	85	MHz
		x7	5	—	85	5	—	85	5	—	85	MHz
		x4	5	—	85	5	—	85	5	—	85	MHz
		x2	5	—	85	5	—	85	5	—	85	MHz
		x1	5	—	170	5	—	170	5	—	170	MHz
HSIODR	Data rate (high-speed I/O performance pin)	x10	100	—	170	100	—	170	100	—	170	Mbps
		x8	80	—	170	80	—	170	80	—	170	Mbps
		x7	70	—	170	70	—	170	70	—	170	Mbps
		x4	40	—	170	40	—	170	40	—	170	Mbps
		x2	20	—	170	20	—	170	20	—	170	Mbps
		x1	10	—	170	10	—	170	10	—	170	Mbps

Symbol	Parameter	Mode	–I6, –C7, –I7			–A7			–C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK}	Input clock frequency (low-speed I/O performance pin)	x10	5	—	85	5	—	85	5	—	85	MHz
		x8	5	—	85	5	—	85	5	—	85	MHz
		x7	5	—	85	5	—	85	5	—	85	MHz
		x4	5	—	85	5	—	85	5	—	85	MHz
		x2	5	—	85	5	—	85	5	—	85	MHz
		x1	5	—	170	5	—	170	5	—	170	MHz
HSIODR	Data rate (low-speed I/O performance pin)	x10	100	—	170	100	—	170	100	—	170	Mbps
		x8	80	—	170	80	—	170	80	—	170	Mbps
		x7	70	—	170	70	—	170	70	—	170	Mbps
		x4	40	—	170	40	—	170	40	—	170	Mbps
		x2	20	—	170	20	—	170	20	—	170	Mbps
		x1	10	—	170	10	—	170	10	—	170	Mbps
t_{DUTY}	Duty cycle on transmitter output clock	—	45	—	55	45	—	55	45	—	55	%
TCCS[42]	Transmitter channel-to-channel skew	—	—	—	340	—	—	340	—	—	340	ps
$t_{x\ Jitter}$	Output jitter (for multi supply devices)	—	—	—	500	—	—	500	—	—	500	ps
t_{RISE}	Rise time	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps

(42) TCCS specifications apply to I/O banks from the same side only.

Symbol	Parameter	Mode	–I6, –C7, –I7			–A7			–C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{FALL}	Fall time	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t_{LOCK}	Time required for the PLL to lock from the end of device configuration.	—	—	—	1	—	—	1	—	—	1	ms

True Mini-LVDS and Emulated Mini-LVDS_E_3R Transmitter Timing Specifications

Table 37: True Mini-LVDS and Emulated Mini-LVDS_E_3R Transmitter Timing Specifications for MAX 10 Dual Supply Devices—Preliminary

True **mini-LVDS** transmitter is only supported at the bottom I/O bank. Emulated **mini-LVDS_E_3R** transmitter is supported at the output pin of all I/O banks.

Symbol	Parameter	Mode	–I6, –C7, –I7			–A7			–C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK}	Input clock frequency (high-speed I/O performance pin)	x10	5	—	155	5	—	150	5	—	155	MHz
		x8	5	—	155	5	—	150	5	—	155	MHz
		x7	5	—	155	5	—	150	5	—	155	MHz
		x4	5	—	155	5	—	150	5	—	155	MHz
		x2	5	—	155	5	—	150	5	—	155	MHz
		x1	5	—	310	5	—	300	5	—	310	MHz

Symbol	Parameter	Mode	–I6, –C7, –I7			–A7			–C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
HSIODR	Data rate (high-speed I/O performance pin)	x10	100	—	310	100	—	300	100	—	310	Mbps
		x8	80	—	310	80	—	300	80	—	310	Mbps
		x7	70	—	310	70	—	300	70	—	310	Mbps
		x4	40	—	310	40	—	300	40	—	310	Mbps
		x2	20	—	310	20	—	300	20	—	310	Mbps
		x1	10	—	310	10	—	300	10	—	310	Mbps
f_{HSCLK}	Input clock frequency (low-speed I/O performance pin)	x10	5	—	150	5	—	145	5	—	150	MHz
		x8	5	—	150	5	—	145	5	—	150	MHz
		x7	5	—	150	5	—	145	5	—	150	MHz
		x4	5	—	150	5	—	145	5	—	150	MHz
		x2	5	—	150	5	—	145	5	—	150	MHz
		x1	5	—	300	5	—	290	5	—	300	MHz
HSIODR	Data rate (low-speed I/O performance pin)	x10	100	—	300	100	—	290	100	—	300	Mbps
		x8	80	—	300	80	—	290	80	—	300	Mbps
		x7	70	—	300	70	—	290	70	—	300	Mbps
		x4	40	—	300	40	—	290	40	—	300	Mbps
		x2	20	—	300	20	—	290	20	—	300	Mbps
		x1	10	—	300	10	—	290	10	—	300	Mbps
t_{DUTY}	Duty cycle on transmitter output clock	—	45	—	55	45	—	55	45	—	55	%

Symbol	Parameter	Mode	–I6, –C7, –I7			–A7			–C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
TCCS[43]	Transmitter channel-to-channel skew	—	—	—	340	—	—	340	—	—	340	ps
$t_{x\ Jitter}$	Output jitter (for multi supply devices)	—	—	—	500	—	—	500	—	—	500	ps
t_{RISE}	Rise time	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t_{FALL}	Fall time	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t_{LOCK}	Time required for the PLL to lock from the end of device configuration.	—	—	—	1	—	—	1	—	—	1	ms

[43] TCCS specifications apply to I/O banks from the same side only.

True LVDS Transmitter Timing

Single Supply Devices True LVDS Transmitter Timing Specifications

Table 38: True LVDS Transmitter Timing Specifications for MAX 10 Single Supply Devices—Preliminary

True **LVDS** transmitter is only supported at the bottom I/O bank.

Symbol	Parameter	Mode	–C7, –I7			–A7			–C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK}	Input clock frequency	x10	5	—	145	5	—	97.5	5	—	100	MHz
		x8	5	—	145	5	—	97.5	5	—	100	MHz
		x7	5	—	145	5	—	97.5	5	—	100	MHz
		x4	5	—	145	5	—	97.5	5	—	100	MHz
		x2	5	—	145	5	—	97.5	5	—	100	MHz
		x1	5	—	290	5	—	195	5	—	200	MHz
HSIODR	Data rate	x10	100	—	290	100	—	195	100	—	200	Mbps
		x8	80	—	290	80	—	195	80	—	200	Mbps
		x7	70	—	290	70	—	195	70	—	200	Mbps
		x4	40	—	290	40	—	195	40	—	200	Mbps
		x2	20	—	290	20	—	195	20	—	200	Mbps
		x1	10	—	290	10	—	195	10	—	200	Mbps
t_{DUTY}	Duty cycle on transmitter output clock	—	45	—	55	45	—	55	45	—	55	%
TCCS[44]	Transmitter channel-to-channel skew	—	—	—	340	—	—	340	—	—	340	ps
$t_{x\ Jitter}$	Output jitter	—	—	—	1,000	—	—	1,000	—	—	1,000	ps

[44] TCCS specifications apply to I/O banks from the same side only.

Symbol	Parameter	Mode	–C7, –I7			–A7			–C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{RISE}	Rise time	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t_{FALL}	Fall time	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t_{LOCK}	Time required for the PLL to lock from the end of device configuration.	—	—	—	1	—	—	1	—	—	1	ms

Dual Supply Devices True LVDS Transmitter Timing Specifications

Table 39: True LVDS Transmitter Timing Specifications for MAX 10 Dual Supply Devices—Preliminary

True **LVDS** transmitter is only supported at the bottom I/O bank.

Symbol	Parameter	Mode	–I6, –C7, –I7			–A7			–C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK}	Input clock frequency	x10	5	—	360	5	—	310	5	—	320	MHz
		x8	5	—	360	5	—	310	5	—	320	MHz
		x7	5	—	360	5	—	310	5	—	320	MHz
		x4	5	—	360	5	—	310	5	—	320	MHz
		x2	5	—	360	5	—	310	5	—	320	MHz
		x1	5	—	360	5	—	310	5	—	320	MHz

Symbol	Parameter	Mode	–I6, –C7, –I7			–A7			–C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
HSIODR	Data rate	x10	100	—	720	100	—	620	100	—	640	Mbps
		x8	80	—	720	80	—	620	80	—	640	Mbps
		x7	70	—	720	70	—	620	70	—	640	Mbps
		x4	40	—	720	40	—	620	40	—	640	Mbps
		x2	20	—	720	20	—	620	20	—	640	Mbps
		x1	10	—	360	10	—	310	10	—	320	Mbps
t_{DUTY}	Duty cycle on transmitter output clock	—	45	—	55	45	—	55	45	—	55	%
TCCS[45]	Transmitter channel-to-channel skew	—	—	—	340	—	—	340	—	—	340	ps
$t_{x\ Jitter}$	Output jitter	—	—	—	500	—	—	500	—	—	500	ps
t_{RISE}	Rise time	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t_{FALL}	Fall time	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t_{LOCK}	Time required for the PLL to lock from the end of device configuration.	—	—	—	1	—	—	1	—	—	1	ms

[45] TCCS specifications apply to I/O banks from the same side only.

Emulated LVDS_E_3R, SLVS, and Sub-LVDS Transmitter Timing Specifications

Single Supply Devices Emulated LVDS_E_3R Transmitter Timing Specifications

Table 40: Emulated LVDS_E_3R Transmitter Timing Specifications for MAX 10 Single Supply Devices—Preliminary

Emulated **LVDS_E_3R** transmitters are supported at the output pin of all I/O banks.

Symbol	Parameter	Mode	–C7, –I7			–A7			–C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK}	Input clock frequency (high-speed I/O performance pin)	x10	5	—	142.5	5	—	97.5	5	—	100	MHz
		x8	5	—	142.5	5	—	97.5	5	—	100	MHz
		x7	5	—	142.5	5	—	97.5	5	—	100	MHz
		x4	5	—	142.5	5	—	97.5	5	—	100	MHz
		x2	5	—	142.5	5	—	97.5	5	—	100	MHz
		x1	5	—	285	5	—	195	5	—	200	MHz
HSIODR	Data rate (high-speed I/O performance pin)	x10	100	—	285	100	—	195	100	—	200	Mbps
		x8	80	—	285	80	—	195	80	—	200	Mbps
		x7	70	—	285	70	—	195	70	—	200	Mbps
		x4	40	—	285	40	—	195	40	—	200	Mbps
		x2	20	—	285	20	—	195	20	—	200	Mbps
		x1	10	—	285	10	—	195	10	—	200	Mbps
f_{HSCLK}	Input clock frequency (low-speed I/O performance pin)	x10	5	—	100	5	—	100	5	—	100	MHz
		x8	5	—	100	5	—	100	5	—	100	MHz
		x7	5	—	100	5	—	100	5	—	100	MHz
		x4	5	—	100	5	—	100	5	—	100	MHz
		x2	5	—	100	5	—	100	5	—	100	MHz
		x1	5	—	200	5	—	200	5	—	200	MHz

Symbol	Parameter	Mode	–C7, –I7			–A7			–C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
HSIODR	Data rate (low-speed I/O performance pin)	x10	100	—	200	100	—	200	100	—	200	Mbps
		x8	80	—	200	80	—	200	80	—	200	Mbps
		x7	70	—	200	70	—	200	70	—	200	Mbps
		x4	40	—	200	40	—	200	40	—	200	Mbps
		x2	20	—	200	20	—	200	20	—	200	Mbps
		x1	10	—	200	10	—	200	10	—	200	Mbps
t_{DUTY}	Duty cycle on transmitter output clock	—	45	—	55	45	—	55	45	—	55	%
TCCS[46]	Transmitter channel-to-channel skew	—	—	—	340	—	—	340	—	—	340	ps
$t_{x\ Jitter}$	Output jitter	—	—	—	1,000	—	—	1,000	—	—	1,000	ps
t_{RISE}	Rise time	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t_{FALL}	Fall time	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t_{LOCK}	Time required for the PLL to lock from the end of device configuration.	—	—	—	1	—	—	1	—	—	1	ms

[46] TCCS specifications apply to I/O banks from the same side only.

Dual Supply Devices Emulated LVDS_E_3R, SLVS, and Sub-LVDS Transmitter Timing Specifications

Table 41: Emulated LVDS_E_3R, SLVS, and Sub-LVDS Transmitter Timing Specifications for MAX 10 Dual Supply Devices—Preliminary

Emulated **LVDS_E_3R**, **SLVS**, and **Sub-LVDS** transmitters are supported at the output pin of all I/O banks.

Symbol	Parameter	Mode	–I6, –C7, –I7			–A7			–C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK}	Input clock frequency (high-speed I/O performance pin)	x10	5	—	300	5	—	267.5	5	—	275	MHz
		x8	5	—	300	5	—	267.5	5	—	275	MHz
		x7	5	—	300	5	—	267.5	5	—	275	MHz
		x4	5	—	300	5	—	267.5	5	—	275	MHz
		x2	5	—	300	5	—	267.5	5	—	275	MHz
		x1	5	—	300	5	—	267.5	5	—	275	MHz
HSIODR	Data rate (high-speed I/O performance pin)	x10	100	—	600	100	—	535	100	—	550	Mbps
		x8	80	—	600	80	—	535	80	—	550	Mbps
		x7	70	—	600	70	—	535	70	—	550	Mbps
		x4	40	—	600	40	—	535	40	—	550	Mbps
		x2	20	—	600	20	—	535	20	—	550	Mbps
		x1	10	—	300	10	—	267.5	10	—	275	Mbps
f_{HSCLK}	Input clock frequency (low-speed I/O performance pin)	x10	5	—	150	5	—	145	5	—	150	MHz
		x8	5	—	150	5	—	145	5	—	150	MHz
		x7	5	—	150	5	—	145	5	—	150	MHz
		x4	5	—	150	5	—	145	5	—	150	MHz
		x2	5	—	150	5	—	145	5	—	150	MHz
		x1	5	—	300	5	—	290	5	—	300	MHz

Symbol	Parameter	Mode	–I6, –C7, –I7			–A7			–C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
HSIODR	Data rate (low-speed I/O performance pin)	x10	100	—	300	100	—	290	100	—	300	Mbps
		x8	80	—	300	80	—	290	80	—	300	Mbps
		x7	70	—	300	70	—	290	70	—	300	Mbps
		x4	40	—	300	40	—	290	40	—	300	Mbps
		x2	20	—	300	20	—	290	20	—	300	Mbps
		x1	10	—	300	10	—	290	10	—	300	Mbps
t_{DUTY}	Duty cycle on transmitter output clock	—	45	—	55	45	—	55	45	—	55	%
TCCS[47]	Transmitter channel-to-channel skew	—	—	—	340	—	—	340	—	—	340	ps
$t_{x\ Jitter}$	Output jitter	—	—	—	500	—	—	500	—	—	500	ps
t_{RISE}	Rise time	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t_{FALL}	Fall time	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t_{LOCK}	Time required for the PLL to lock from the end of device configuration.	—	—	—	1	—	—	1	—	—	1	ms

[47] TCCS specifications apply to I/O banks from the same side only.

LVDS, TMDS, HiSpi, SLVS, and Sub-LVDS Receiver Timing Specifications

Single Supply Devices LVDS Receiver Timing Specifications

Table 42: LVDS Receiver Timing Specifications for MAX 10 Single Supply Devices—Preliminary

LVDS receivers are supported at all banks.

Symbol	Parameter	Mode	–C7, –I7		–A7		–C8		Unit
			Min	Max	Min	Max	Min	Max	
f_{HSCLK}	Input clock frequency (high-speed I/O performance pin)	x10	5	145	5	97.5	5	100	MHz
		x8	5	145	5	97.5	5	100	MHz
		x7	5	145	5	97.5	5	100	MHz
		x4	5	145	5	97.5	5	100	MHz
		x2	5	145	5	97.5	5	100	MHz
		x1	5	290	5	195	5	200	MHz
HSIODR	Data rate (high-speed I/O performance pin)	x10	100	290	100	195	100	200	Mbps
		x8	80	290	80	195	80	200	Mbps
		x7	70	290	70	195	70	200	Mbps
		x4	40	290	40	195	40	200	Mbps
		x2	20	290	20	195	20	200	Mbps
		x1	10	290	10	195	10	200	Mbps
f_{HSCLK}	Input clock frequency (low-speed I/O performance pin)	x10	5	100	5	100	5	100	MHz
		x8	5	100	5	100	5	100	MHz
		x7	5	100	5	100	5	100	MHz
		x4	5	100	5	100	5	100	MHz
		x2	5	100	5	100	5	100	MHz
		x1	5	200	5	200	5	200	MHz

Symbol	Parameter	Mode	–C7, –I7		–A7		–C8		Unit
			Min	Max	Min	Max	Min	Max	
HSIODR	Data rate (low-speed I/O performance pin)	x10	100	200	100	200	100	200	Mbps
		x8	80	200	80	200	80	200	Mbps
		x7	70	200	70	200	70	200	Mbps
		x4	40	200	40	200	40	200	Mbps
		x2	20	200	20	200	20	200	Mbps
		x1	10	200	10	200	10	200	Mbps
SW	Sampling window	—	—	700	—	700	—	700	ps
$t_{x\ Jitter}$	Input jitter	—	—	1,000	—	1,000	—	1,000	ps
t_{LOCK}	Time required for the PLL to lock from the end of device configuration.	—	—	1	—	1	—	1	ms

Dual Supply Devices LVDS, TMDS, HiSpi, SLVS, and Sub-LVDS Receiver Timing Specifications

Table 43: LVDS, TMDS, HiSpi, SLVS, and Sub-LVDS Receiver Timing Specifications for MAX 10 Dual Supply Devices—Preliminary

LVDS, **TMDS**, **HiSpi**, **SLVS**, and **Sub-LVDS** receivers are supported at all banks.

Symbol	Parameter	Mode	–I6, –C7, –I7		–A7		–C8		Unit
			Min	Max	Min	Max	Min	Max	
f_{HSCLK}	Input clock frequency (high-speed I/O performance pin)	x10	5	360	5	310	5	320	MHz
		x8	5	360	5	310	5	320	MHz
		x7	5	360	5	310	5	320	MHz
		x4	5	360	5	310	5	320	MHz
		x2	5	360	5	310	5	320	MHz
		x1	5	360	5	310	5	320	MHz

Symbol	Parameter	Mode	–I6, –C7, –I7		–A7		–C8		Unit
			Min	Max	Min	Max	Min	Max	
HSIODR	Data rate (high-speed I/O performance pin)	x10	100	720	100	620	100	640	Mbps
		x8	80	720	80	620	80	640	Mbps
		x7	70	720	70	620	70	640	Mbps
		x4	40	720	40	620	40	640	Mbps
		x2	20	720	20	620	20	640	Mbps
		x1	10	360	10	310	10	320	Mbps
f_{HSCLK}	Input clock frequency (low-speed I/O performance pin)	x10	5	150	5	145	5	150	MHz
		x8	5	150	5	145	5	150	MHz
		x7	5	150	5	145	5	150	MHz
		x4	5	150	5	145	5	150	MHz
		x2	5	150	5	145	5	150	MHz
		x1	5	300	5	290	5	300	MHz
HSIODR	Data rate (low-speed I/O performance pin)	x10	100	300	100	290	100	300	Mbps
		x8	80	300	80	290	80	300	Mbps
		x7	70	300	70	290	70	300	Mbps
		x4	40	300	40	290	40	300	Mbps
		x2	20	300	20	290	20	300	Mbps
		x1	10	300	10	290	10	300	Mbps
SW	Sampling window	—	—	400	—	400	—	400	ps
$t_{x\ Jitter}$	Input jitter	—	—	500	—	500	—	500	ps
t_{LOCK}	Time required for the PLL to lock from the end of device configuration.	—	—	1	—	1	—	1	ms

Memory Output Clock Jitter Specifications

MAX 10 devices support external memory interfaces up to 300 MHz. The external memory interfaces for MAX 10 devices calibrate automatically.

The memory output clock jitter measurements are for 200 consecutive clock cycles.

The clock jitter specification applies to memory output clock pins generated using DDIO circuits clocked by a PLL output routed on a global clock network.

DDR3 and LPDDR2 SDRAM memory interfaces are only supported on the fast speed grade device.

Table 44: Memory Output Clock Jitter Specifications for MAX 10 Devices—Preliminary

Parameter	Symbol	–6 Speed Grade		–7 Speed Grade		Unit
		Min	Max	Min	Max	
Clock period jitter	$t_{JIT(per)}$	–100	100	–125	125	ps
Cycle-to-cycle period jitter	$t_{JIT(cc)}$	—	200	—	250	ps

Related Information

Literature: External Memory Interfaces

Provides more information about external memory system performance specifications, board design guidelines, timing analysis, simulation, and debugging information.

Configuration Specifications

This section provides configuration specifications and timing for MAX 10 devices.

JTAG Timing Parameters

Table 45: JTAG Timing Parameters for MAX 10 Devices—Preliminary

The values are based on C_L = 10 pF of TDO .

The affected Boundary Scan Test (BST) instructions are SAMPLE/PRELOAD, EXTEST, INTEST, and CHECK_STATUS.

Symbol	Parameter	Non-BST and non-CONFIG_IO Operation		BST and CONFIG_IO Operation		Unit
		Minimum	Maximum	Minimum	Maximum	
t_{JCP}	TCK clock period	40	—	50	—	ns
t_{JCH}	TCK clock high time	20	—	25	—	ns
t_{JCL}	TCK clock low time	20	—	25	—	ns
t_{JPSU_TDI}	JTAG port setup time	2	—	2	—	ns
t_{JPSU_TMS}	JTAG port setup time	3	—	3	—	ns
t_{JPH}	JTAG port hold time	10	—	10	—	ns
t_{JPCO}	JTAG port clock to output	—	• 15 (for V_{CCIO} = 3.3, 3.0, and 2.5 V) • 17 (for V_{CCIO} = 1.8 and 1.5 V)	—	• 18 (for V_{CCIO} = 3.3, 3.0, and 2.5 V) • 20 (for V_{CCIO} = 1.8 and 1.5 V)	ns
t_{JPZX}	JTAG port high impedance to valid output	—	• 15 (for V_{CCIO} = 3.3, 3.0, and 2.5 V) • 17 (for V_{CCIO} = 1.8 and 1.5 V)	—	• 15 (for V_{CCIO} = 3.3, 3.0, and 2.5 V) • 17 (for V_{CCIO} = 1.8 and 1.5 V)	ns
t_{JPXZ}	JTAG port valid output to high impedance	—	• 15 (for V_{CCIO} = 3.3, 3.0, and 2.5 V) • 17 (for V_{CCIO} = 1.8 and 1.5 V)	—	• 15 (for V_{CCIO} = 3.3, 3.0, and 2.5 V) • 17 (for V_{CCIO} = 1.8 and 1.5 V)	ns

POR Specifications

Table 46: POR Delay Specifications for MAX 10 Devices—Preliminary

POR Delay	Condition	Minimum	Maximum	Unit
Don't Care	Instant-on enabled	No delay		—
Fast	Instant-on disabled	3	9	ms
Standard	Instant-on disabled	50	200	ms

Remote System Upgrade Circuitry Timing Specifications

Table 47: Remote System Upgrade Circuitry Timing Specifications for MAX 10 Devices—Preliminary

Parameter	Minimum	Maximum	Unit
$t_{MAX\_RU\_CLK}$	—	40	MHz
$t_{RU\_nCONFIG}$	250	—	ns
$t_{RU\_nRSTIMER}$	250	—	ns

User Watchdog Internal Circuitry Timing Specifications

Table 48: User Watchdog Timer Specifications for MAX 10 Devices—Preliminary

The specifications are subject to PVT changes.

Parameter	Device	Minimum	Typical	Maximum	Unit
User watchdog internal oscillator frequency	10M02, 10M04, 10M08, 10M16, 10M25	3.4	5.1	7.3	MHz
	10M40, 10M50	2.2	3.3	4.8	MHz

Uncompressed Raw Binary File (.rbf) Sizes

Table 49: Uncompressed .rbf Sizes and Internal Configuration Time for MAX 10 Devices—Preliminary

The internal configuration time is based on the uncompressed, unencrypted, and without memory initialization files. Turn on instant-on feature to measure the internal configuration time. The internal configuration time measurement is from the minimum value of V_{CC_ONE} (for single supply devices) or V_{CC} (for dual supply devices) to user mode entry.

Device	CFM Data Size (bits)		Internal Configuration Time (ms)
	Without Memory Initialization	With Memory Initialization	
10M02	554,000	676,000	3
10M04	1,540,000	1,880,000	4
10M08	1,540,000	1,880,000	4
10M16	2,800,000	3,430,000	5
10M25	4,140,000	4,780,000	5
10M40	7,840,000	9,670,000	9
10M50	7,840,000	9,670,000	9

Related Information

MAX 10 FPGA Configuration User Guide
Provides more information about instant-on feature.

Glossary

Table 50: Glossary

Letter	Subject	Definition
A	—	—
B	—	—
C	—	—

Letter	Subject	Definition
D	—	—
E	—	—
F	—	—
G	—	—
H	—	—
I	—	—
J	—	—
K	—	—
L	—	—
M	—	—
N	—	—
O	—	—
P	Preliminary	Some tables show the designation as "Preliminary". Preliminary characteristics are created using simulation results, process data, and other known parameters. Final numbers are based on actual silicon characterization and testing. The numbers reflect the actual performance of the device under worst-case silicon process, voltage, and junction temperature conditions. There are no preliminary designations on finalized tables.
Q	—	—
R	R_L	Receiver differential input discrete resistor (external to MAX 10 devices).
	RSKM (Receiver input skew margin)	HIGH-SPEED I/O block: The total margin left after accounting for the sampling window and TCCS. RSKM = (TUI – SW – TCCS) / 2.

Letter	Subject	Definition
S	Sampling window (SW)	HIGH-SPEED I/O Block: The period of time during which the data must be valid to capture it correctly. The setup and hold times determine the ideal strobe position in the sampling window.
	Single-ended voltage referenced I/O standard	The AC input signal values indicate the voltage levels at which the receiver must meet its timing specifications. The DC input signal values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input crosses the AC value, the receiver changes to the new logic state. The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing.

Letter	Subject	Definition
T	t_C	High-speed receiver/transmitter input and output clock period.
	TCCS (Channelto- channel-skew)	HIGH-SPEED I/O block: The timing difference between the fastest and slowest output edges, including t_{CO} variation and clock skew. The clock is included in the TCCS measurement.
	t_{cin}	Delay from clock pad to I/O input register.
	t_{CO}	Delay from clock pad to I/O output.
	t_{cout}	Delay from clock pad to I/O output register.
	t_{DUTY}	HIGH-SPEED I/O Block: Duty cycle on high-speed transmitter output clock.
	t_{FALL}	Signal high-to-low transition time (80–20%).
	t_H	Input register hold time.
	Timing Unit Interval (TUI)	HIGH-SPEED I/O block: The timing budget allowed for skew, propagation delays, and data sampling window. (TUI = 1/(Receiver Input Clock Frequency Multiplication Factor) = t_C/w).
	$t_{INJITTER}$	Period jitter on PLL clock input.
	$t_{OUTJITTER\_DEDCLK}$	Period jitter on dedicated clock output driven by a PLL.
	$t_{OUTJITTER\_IO}$	Period jitter on general purpose I/O driven by a PLL.
	t_{pllcin}	Delay from PLL inclk pad to I/O input register.
	$t_{pllcout}$	Delay from PLL inclk pad to I/O output register.
	t_{RISE}	Signal low-to-high transition time (20–80%).
	t_{SU}	Input register setup time.
U	—	—
V	$V_{CM(DC)}$	DC common mode input voltage.
	$V_{DIF(AC)}$	AC differential input voltage: The minimum AC input differential voltage required for switching.
	$V_{DIF(DC)}$	DC differential input voltage: The minimum DC input differential voltage required for switching.
	V_{ICM}	Input common mode voltage: The common mode of the differential signal at the receiver.
	V_{ID}	Input differential Voltage Swing: The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.

Letter	Subject	Definition
	V_{IH}	Voltage input high: The minimum positive voltage applied to the input which is accepted by the device as a logic high.
	$V_{IH(AC)}$	High-level AC input voltage.
	$V_{IH(DC)}$	High-level DC input voltage.
	V_{IL}	Voltage input low: The maximum positive voltage applied to the input which is accepted by the device as a logic low.
	$V_{IL\ (AC)}$	Low-level AC input voltage.
	$V_{IL\ (DC)}$	Low-level DC input voltage.
	V_{IN}	DC input voltage.
	V_{OCM}	Output common mode voltage: The common mode of the differential signal at the transmitter.
	V_{OD}	Output differential voltage swing: The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter. $V_{OD} = V_{OH} - V_{OL}$.
	V_{OH}	Voltage output high: The maximum positive voltage from an output which the device considers is accepted as the minimum positive high level.
	V_{OL}	Voltage output low: The maximum positive voltage from an output which the device considers is accepted as the maximum positive low level.
	V_{OS}	Output offset voltage: $V_{OS} = (V_{OH} + V_{OL}) / 2$.
	$V_{OX\ (AC)}$	AC differential Output cross point voltage: The voltage at which the differential output signals must cross.
	V_{REF}	Reference voltage for SSTL, HSTL, and HSUL I/O Standards.
	$V_{REF(AC)}$	AC input reference voltage for SSTL, HSTL, and HSUL I/O Standards. $V_{REF(AC)} = V_{REF(DC)}$ + noise. The peak-to-peak AC noise on V_{REF} should not exceed 2% of $V_{REF(DC)}$.
	$V_{REF(DC)}$	DC input reference voltage for SSTL, HSTL, and HSUL I/O Standards.
	$V_{SWING\ (AC)}$	AC differential input voltage: AC Input differential voltage required for switching.
	$V_{SWING\ (DC)}$	DC differential input voltage: DC Input differential voltage required for switching.
	V_{TT}	Termination voltage for SSTL, HSTL, and HSUL I/O Standards.

Letter	Subject	Definition
	$V_{X\ (AC)}$	AC differential Input cross point voltage: The voltage at which the differential input signals must cross.
W	—	—
X	—	—
Y	—	—
Z	—	—

Document Revision History for MAX 10 FPGA Device Datasheet

Date	Version	Changes
September 2014	2014.09.22	Initial release.